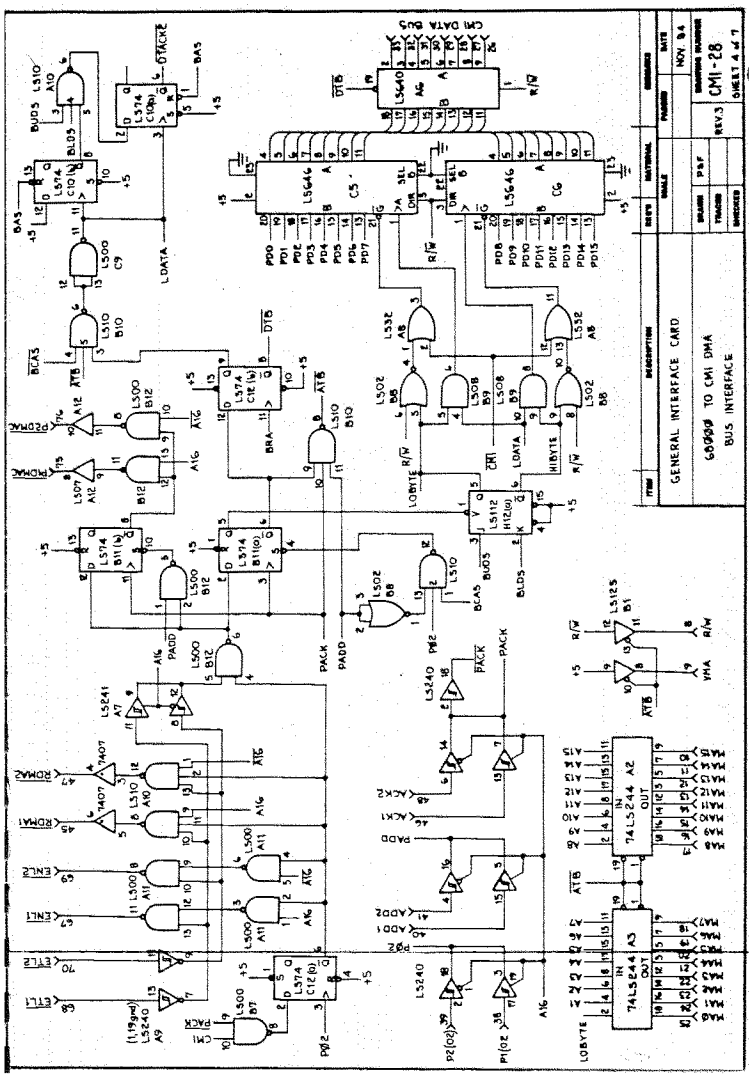



# FAIRLIGHT

## COMPUTER MUSICAL INSTRUMENT

# CMI SYSTEM SERVICE MANUAL

# CMI SYSTEM SERVICE MANUAL

FAIRLIGHT INSTRUMENTS, JUNE 1982

## SECTION 1. INTRODUCTION TO C.M.I. MAINFRAME

### 1.0 INTRODUCTION

The Fairlight Computer Musical Instrument is a complete music production and performance instrument. It is a special purpose computer system incorporating a custom dual M6800 central processor interfaced to special input-output devices optimised for the rather unusual requirements of music production.

The information presented in this manual is intended as a guide to give the reader an appreciation of the general operating principles of the C.M.I. In the event of a malfunction, it should be used to isolate which of the four main C.M.I. sub-systems is at fault, then for detailed functional information refer to the service manual for the item concerned.

Related documents are: C.M.I. MAINFRAME SERVICE MANUAL
GRAPHICS TERMINAL SERVICE MANUAL
ALPHA-NUMERIC KEYBOARD SERVICE MANUAL
MUSIC KEYBOARD SERVICE MANUAL
FLOPPY-DISK DRIVE SERVICE MANUAL

### 1.1 SYSTEM OVERVIEW

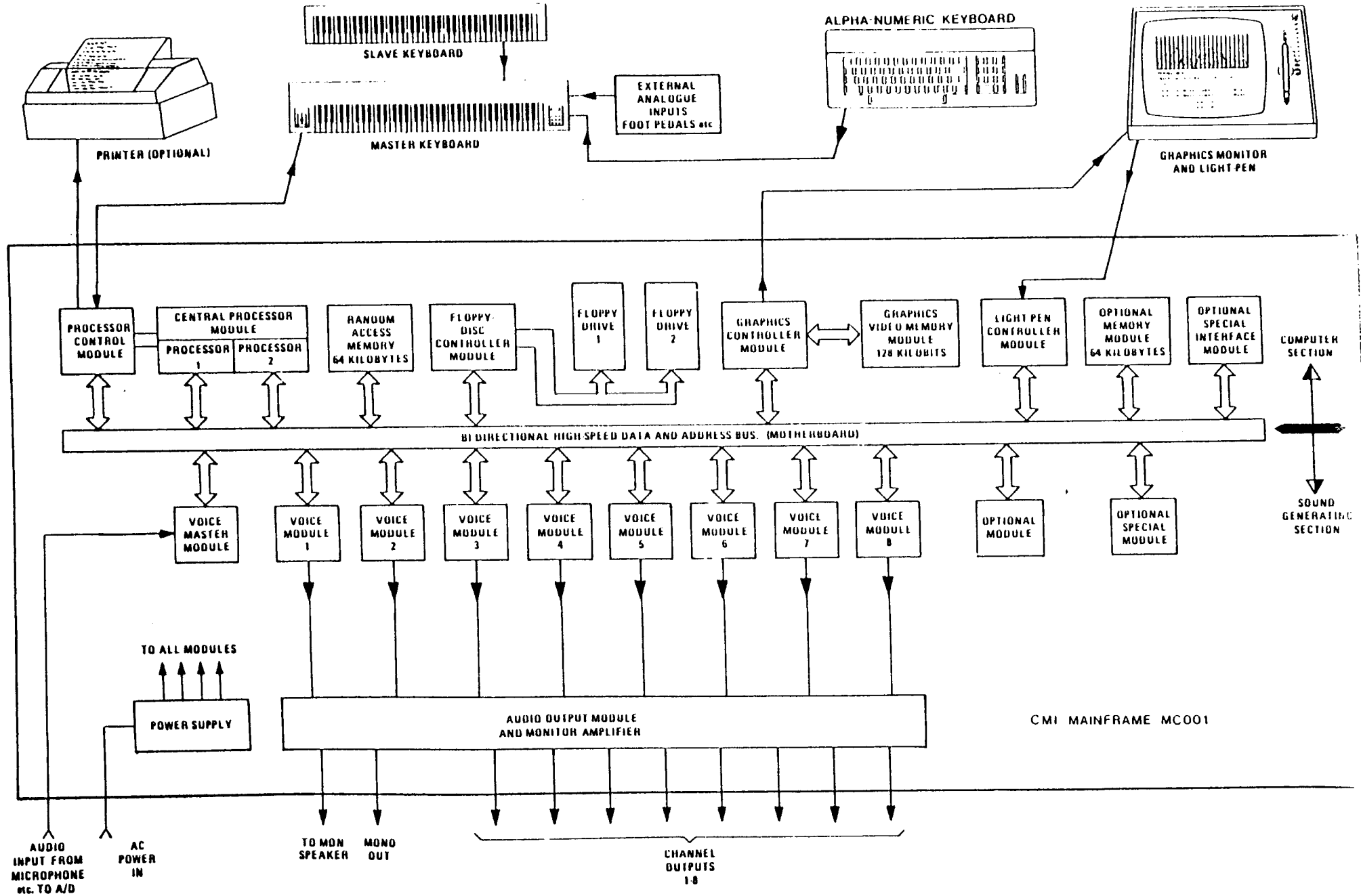
The system comprises for main units (Refer Fig. 1).

1) Mainframe: Houses the computer section, floppy disk drives, audio generation section and power supplies.

2) Graphics Terminal: The primary display terminal for the computer. It is a 15 inch C.R.T. display with lightpen.

3) Alphanumeric Keyboard: Sends serial ASCII data to the computer. Used for operator input of commands etc.

4) Music Keyboard: Piano-like keyboard sends serial data to the computer on each key depression. Used for live playing. Also includes several analog controls and switches which are digitised, and a numeric keypad with 12 character alpha-numeric display which serves as a secondary Input-Output device.



## SECTION 2. FUNCTIONAL DESCRIPTION

### 2.1 C.M.I. MAINFRAME

The Mainframe houses the computer section of the C.M.I., that is all the digital control and sound generating hardware. It can be considered a stand-alone operational unit. With nothing connected to it it is possible to start up the system and bootstrap load the disks (BOOT the system). On power-up, EPROMS located on the C.P.U. Control Card Q-032 will control the Boot process.

As soon as a disk is placed in the left-hand drive (Drive 0) a special sector known as the Boot Block is read into RAM and executed. The code in the Boot Block then completes the Boot by reading in the C.M.I. Operating System. The system is then ready to accept commands from the alpha-keyboard, music keyboard or light pen.

For deatailed information refer to the C.M.I. MAINFRAME SERVICE MANUAL.

### 2.2 GRAPHICS TERMINAL

Display data for the Graphics Terminal is generated by the Graphics Display card Q-045 in the form of a composite video signal. The display format is a bit-mapped image of 16 kilobytes of VRAM, displayed as a 512 (Horizontal) by 256 (Vertical) matrix.

The Light-Pen operates by sending a pulse back to the computer when the phosphor dot is "seen" to flash past. The Light Pen Interface Q-148, located in the Mainframe generates X-Y co-ordinates from the timing of this pulse. As well as this "Hit" signal from the lightpen, there is a "Touch" signal, which indicates that the operator has activated the pen by touching the end.

For detailed information, refer to the GRAPHICS TERMINAL SERVICE MANUAL.

### 2.3 MUSIC KEYBOARD

The music keyboard interfaces to the Mainframe via a bi-directional RS-232C port located on the processor control card Q-032. The Baud rate is selected by the Terminal Speed control on the from panel of the mainframe, and D.I.L. switches inside the keyboard. Both of these must be set to 9600 Baud.

The keyboard is controlled by an on-card M6802 microprocessor executing a program in EPROM. As well as data communications with the Mainframe, data coming in from the alpha-numeric keyboard is pre-processed before being forwarded to the mainframe.

Data is sent to the computer whenever:

1) A music key is depressed or released
3) A key on the alpha keyboard is pressed
3) One of the three faders is moved
4) A switch or pedal plugged into the keyboard is operated

Keystroke data is sent in the form of three-byte packets. This includes keyboard number, key number, depression/release flag and key velocity data. Key velocity is calculated by the on-card processor which times the flight of the key contact as it travels between two busbars.

The 12 digit alpha-numeric display on the right-hand end of the keyboard is used to display messages to the operator in circumstances where the Graphics Terminal is not being used. The display is controlled by the processor on the keyboard. On power-up, the message - POWER ON - is displayed. This is generated locally by the keyboard itself. Once Booting has commenced, the message LOADING is dispalyed. This message is sent by the mainframe, via the serial link.

The control devices (faders, switches and pedals) are digitised by an eight-bit Analogue to Digital converter in the music keyboard and when the data changes, a packet of data is transmitted down the serial link to the mainframe.

For detailed information, refer to the MUSIC KEYBOARD SERVICE MANUAL.

## 2.4 ALPHA-NUMERIC KEYBOARD

This keyboard uses another M6802 microprocessor which controls scanning of the 62 Hall-effect switches and serialises the data which is transmitted in ASCII format, RS-232C protocol. Data rate used is 9600 Baud, selected by D.I.L. switches on the circuit board. The processor executes firmware stored in EPROM.

Normally the alpha-numeric keyboard is plugged into the music keyboard. It receives its power from there, and sends its data to the processor in the music keyboard. The data is flagged as alpha-numeric, queued until there is no music keyboard data, and then forwarded to the mainframe. If desired, the alpha keyboard can be plugged directly into the Keyboard connector on the mainframe, bypassing the music keyboard. This can be a useful diagnostic aid.

## 2.5 INTERCONNECTING CABLES

The four major sub-systems are connected by pluggable cable sets which should be treated with the same suspicion warranted by mechanical parts. The signals carried by each cable, together with pin numbers, are described fully in section 4, below.

## SECTION 3. TROUBLESHOOTING

This section covers troubleshooting the C.M.I. system only to the level of identifying which of the four sub-systems (mainframe, music keyboard, alpha-keyboard or graphics terminal) is at fault. Having done this, service personel should refer to the service manual for the offending item.

NOTE: Remember that the C.M.I. is a complex piece of hardware running sophisticated software, and it is sometimes hard to differentiate between a hardware fault, software bug, and operator error. If there is any douot, the same sequence of operations should be tried on a known good system before attempting hardware repairs. In executing the following diagnostic procedures, the serviceman should be aware that a faulty System Disk can cause what appears to be hardware faults. Furthermore, hardware faults can cause disks to be destroyed, either physically or by corrupting data, so it is wise to keep a good supply of C.M.I. system disks and diagnostic disks on hand.

### 3.1 FAULT ISOLATION BY SUB-SYSTEM SUBSTITUTION

The easiset way to identify the faulty sub-system is to exchange whole units for known good ones if such are available. If a complete working system is on hand, exchange each sub-system in turn, starting with the most likely to be responsible for a given fault. Some common fault symptoms and suggested substitution procedures follow.

3.1.1 System will not boot. (Sucessful Boot is indicated by Page 1 appearing on the screen, or Page 1 Ready message at the music keyboard).

Unplug keyboard from mainframe. If it still does not boot, the fault is in the mainframe. If it does boot, try substituting the music keyboard. If it still does not boot, substitute the alpha-keyboard. The Graphics Terminal should not be able to affect booting. If the problem does not go away at any stage, substitute the interconnecting cables one by one.

3.1.2 System boots (Page 1 on screen or message at keyboard) but does not respond to alpha keyboard commands.

Substitute music keyboard, then alpha keyboard, then graphics terminal, then cables. If problem persists, the fault is in the mainframe.

3.1.3 No sound when voice loaded and music keyboard played.

Substitute music keyboard first, then cables, then alpha keybaord, then granics terminal. Plug the alpha-keyboard into the mainframe directly, and hit <CNTRL P>. A note should play. If not, the fault is in the mainframe.

3.1.4 System works properly except Graphics display or lightpen malfunctions.

Substitute graphics terminal and cable first. If no better, fault is almost certainly in mainframe.

3.1.5 Other strange behaviour.

Start by substituting mainframe.

3.2 SUB-SYSTEM CHECKOUT WITHOUT SUBSTITUTION

In many cases the faulty sub-system will have to be identified using only commonly available test equipment. Minimum requirements are a multimeter for measuring volts D.C. and resistance, an oscilloscope, and the usual set of tools such as screw drivers, pliers, soldering iron etc.

The faulty sub-system can usually be isolated by the following tests:

3.2.1 System will not boot.

Unplug keyboard input and try again. If system does not boot, fault is in mainframe. If it now boots, fault is in music keyboard, alpha keyboard or cables. To isolate which, try again with alpha keyboard plugged straight into mainframe to eliminate music keyboard.

3.1.2 System boots but does not respond to alpha keyboard commands.

Most likely fault is in alpha-keyboard or cable. If the keyboard does not click when a key is pressed, either the keyboard is faulty or the power supply to the keyboard has failed. Check the supplies and data output at the keyboard plug using the Signal List (Section 4, below).

3.1.3 No sound when voice loaded and music keyboard played.

Check for normal operation with the alpha-keyboard plugged directly into the mainframe. A note should be heard if <CTRL P> is pressed with a voice loaded. If this works, then the music keyboard or cable is probably faulty. Check for the correct signals at the power and signal connectors at the music keyboard. (Refer section 4).

If there is no sound in response to the <CNTRL P>, then the fault is in the mainframe.

3.1.4 System works properly except Graphics Terminal malfunctions.

Check video ouput signal at the Graphics connector. If this is normal, fault is in Graphics Terminal or cable. Note that a negative image can be caused by a fault in the graphics terminal or the mainframe, and cannot be easily seen by looking at the signal on an oscilloscope. To achieve a substantially black image for examination with the oscilloscope, remove the system disk and restart both processors. This will result in just the words CMI READY on a black screen, in which case the scope display should show any fault clearly.

3.1.5 Lightpen does not work but everything else normal.

Point the lightpen at a light area of the screen. If there is a cursor which disappears when the Touch is activated, then the fault is in the mainframe. Otherwise the fault may be in the Graphics Terminal, lightpen or cables. Check for proper Hit and Touch signals at the Graphics connector at the mainframe by unplugging the cable and using an oscilloscope. If these are not correct the fault is in the Graphics Terminal. Otherwise the mainframe is faulty.

3.1.6 Other strange behaviour.

Most other faults such as improper operation of one or more of the sound channels or unreliable reponse from the computer can be attributed to a fault in the mainframe. To eliminate all other posibilities a useful diagnostic trick is to start the system playing a long M.C.L. or Page 9 Sequencer loop and un-plug all cables except the mains input and audio ouput. If the fault is still evident, then the mainframe is definitely to blame.

This section describes the signals present in each conductor of each interconnecting cable in the C.M.I. System when functioning normally. Refer to Figure 2 for cable identification.

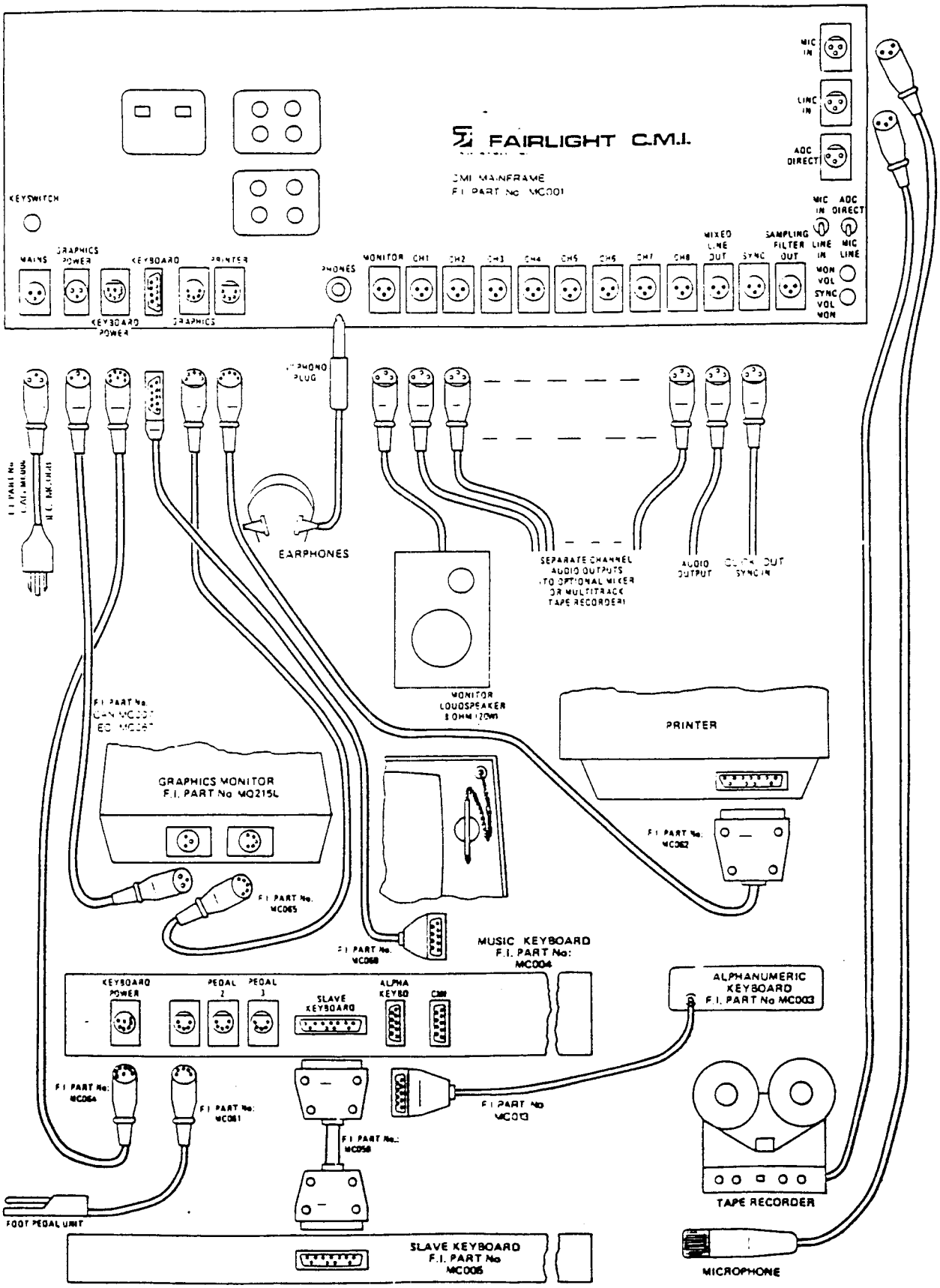



Figure 2 C.M.I. SYSTEM INTERCONNECTION CABLES

4.1 Mains Cable: Part no. MC006 (Cannon) or MC068 (I.E.C.)

A.C. Mains Neutral, Active and Ground.

4.2 Graphics Terminal Power: MC007 (Cannon) or MC067 (I.E.C.)

A.C. Mains supply to Graphics Terminal. Switched by key switch on mainframe. This supply is always the same as the local mains potential.

4.3 Graphics Terminal Signal: MC065

Video signal to Graphics Terminal and Light Pen signals to mainframe.

Connector Type: Cannon 5-pin.

| | |
|---|---|
| Pin 1 | Lightpen Hit. T.T.L. level, asserted low. On oscilloscope, appears as a series of low-going pulses about 1uS wide, repeated every 20mS, when the pen is pointed at a bright area of the screen. (See fig 3a) |
| Pin 2 | Lightpen Signal Return. Ground for lightpen signal cables. |
| Pin 3 | Lightpen Touch. T.T.L. level, asserted low. Normally at approx +4 volts, goes low (less than 0.4 V) when the end of the lightpen touched. |
| Pin 4 | Video Return. Ground for Video signal cable. |
| Pin 5 | Composite Video. 1V P-P video signal to Groaphics display. Format is 625 lines, 50 Hz frame rate. (See fig 3b) |

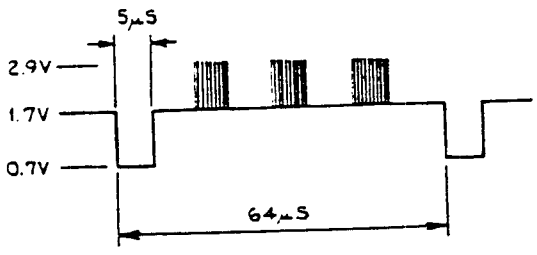



Figure 3a LIGHTPEN HIT SIGNAL

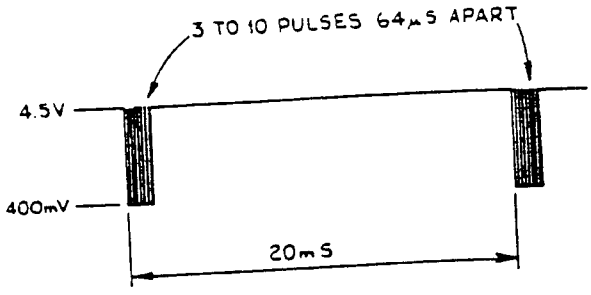



Figure 3 b COMPOSITE VIDEO

4.4 Music Keyboard Power: MC064

Unregulated power supply to music keyboard (also indiectly supplies alphanumeric keyboard).

Connector Type: Cannon 7-pin.

Pins 1,2 +10V Return. Return (ground) for +10V supply.

Pins 3,4 +10V Supply. Unregulated supply, +9 to +11 volts.

Pin 5 -20V Supply. Unregulated supply, -18 to -22 volts.

Pin 6 +20,-20 Return. Return (ground) for + and - 20 supplies.

Pin 7 +20V Supply. Unregulated supply, +18 to +22 volts.

4.5 Music Keyboard Signal: MC060

Bi-directional serial data between mainframe and music keyboard, including "busy" flags in both directions. Power supply is also carried by this cable, to power the alpha-numeric keyboard if it is connected instead of the music keyboard.

Connector Type: 9 Pin "D-Mini"

Pin 1 +18 to 22 volts unregulated supply. This is not used by the music keyboard.

Pin 2 DON1. Signal to enable transmission of data from the keyboard. RS-232 levels. Enabled: >7 volts. Disabled <-7 volts. With nothing being transmitted from the keyboard, this signal should be at approx. +10 volts. When keys are pressed or released a burst of -10 volt pulses should be seen for between 2 and 10 milliseconds.

Pin 3 -18 to -22 volts unregulated supply. This is not used by the music keyboard.

Pin 4 FLAG1. Signal to diasble transmission of data from the mainframe to the keyboard. Signal is normally +10 volts.

Pin 5 SIGNAL RETURN. Ground for data paths.

Pin 6 DATA IN. Serial data from keyboard to mainframe. Format is RS-232. Normally at -10 volts. When a key is pressed or released a burst of +10 volt pulses lasting approx. 3 mS sholud be seen.

Pin 7 POWER RETURN. Return (Ground) for + and - supplies.

Pin 8 Not Connected.

Pin 9 DATA1. Serial data from mainframe to keyboard. Format is RS-232. Normally at -10 volts. For each character sent from the mainframe to the alpha-numeric display a burst of +10 volt pulses lasting approx. 1 mS should be seen.

## 4.6 Alpha-numeric Keyboard Power/Signal : MC013

Unregulated power supplies to alphanumeric keyboard, serial data from alphanumeric keyboard.

Connector Type: 9 Pin "D-Mini"

| | |
|---|---|
| Pin 1 | +18 to 22 volts unregulated supply. |
| Pin 2 | Not Connected. |
| Pin 3 | -18 to -22 volts unregulated supply. |
| Pin 4 | Not Connected. |
| Pin 5 | SIGNAL RETURN. Ground for data paths. |
| Pin 6 | DATA OUT. Serial data from keyboard. Format is RS-232. Normally at -10 volts. Each time a key is pressed a burst of +10 volt pulses lasting approx. 1 mS should be seen. |
| Pin 7 | POWER RETURN. Return (Ground) for + and - supplies. |
| Pin 8 | Not Connected. |
| Pin 9 | Not Connected. |

## 4.7 Slave Keyboard Power/Signal : MC059

The Music Keyboard sends power and key multiplexer addressing data to the slave keyboard. Key data is returned from the slave keyboard.

Connector Type: "D Mini" 25-pin.

| | |
|---|---|
| Pins 1,2 | POWER SUPPLY RETURN. Ground. |
| Pin 3 | KEY ADDRESS 0 Least significant key multiplexer address bit. CMOS logic levels. |
| Pins 4,7 | KEY ADDRESS BITS 1-4. CMOS Logic levels |
| Pin 8 | SIGNAL RETURN Ground. |
| Pin 9 | KEY DATA 1. Data returned from key multiplexer scanning the lowest 24 keys. Normally at approx. -5 volts. Goes to 0 volts while key is in flight, and +5 volts when key is at rest in fully depressed position. |
| Pin 10 | KEY DATA 2. Data from middle 24 keys. |
| Pin 11 | KEY DATA 3. Data from top 25 keys. |

Pins 11-21 Not Connected

Pins 22,23 -20 SUPPLY. Unregulated power supply to slave keyboard, +18 to +22 volts.

Pins 24,25 +20 SUPPLY. Unregulated power supply to slave keyboard, -18 to +22 volts.

4.8 Printer : MC062 9600 BAUD

Serial data from mainframe to printer, "busy" flag from printer to mainframe, plus "device on" signal used to switch on printer in readiness to receive data.

Connector type: Cannon 5 pin.

Pin 1 Signal Ground.

Pin 2 Not Connected.

Pin 3 FLAGO. "Busy" flag from printer. RS-232 levels. <-7 volts when printer ready, >+7 volts when printer busy.

Pin 4 DONO. "Device On" control from mainframe to printer. RS-232 level, >+7 volts to enable printer, <-7 volts to diable printer. This signal is optional as some printers do not require it.

Pin 5 DATAO. Serial data to printer. RS-232 levels, ASCII format. Normally at -10 volts. For each character sent from the mainframe to the printer a burst of +10 volt pulses lasting approx. 1 mS should be seen.

4.9 Phones

Output for driving headphones. Monitors the MIXED LINE output. Internally, this output is taken from the MONITOR (speaker) output via a 100 ohm resistor.

Connector type: 1/4" (6.25 MM) stereo phono jack.

The following signal lists refer to connectors on the rear of the C.M.I. Mainframe.

4.10 Monitor

Output for driving a monitor speaker. The internal monitor amplifier will deliver a maximum of 20 watts R.M.S. into an 8 ohm speaker. Note that the Mainframe is fitted with a 1 amp speaker fuse which will blow if the monitor amplifier is driven to full output under load for more than a second.

Connector Type: Cannon 3 pin.

Pins 1,2 Ground

Pin 3 Active. With all channels producing a full-amplitude sinewave and the MONITOR control turned up to the point of clipping, this output should be approx. 38 volts P-P (with no load)

4.11 Channels 1-8

Individual channel outputs (balanced, 600 ohms impedance).

Connector type: Cannon 3 pin.

Pin 1 Ground

Pin 2 Output Cold. Anti-phase output, maximum level 3.7 volts P-P.

Pin 3 Output Hot. Maximum level 3.7 volts P-P.

4.12 Mixed Line Output

Mixed output of all eight channels (balanced, 600 ohms impedance).

Connector Type: Cannon 3-Pin

Pin 1 Ground

Pin 2 Output Cold. Anti-phase output, maximum level 3.7 volts P-P.

Pin 3 Output Hot. Maximum level 3.7 volts P-P.

4.13 Sync

Synchronising input and output, for use with Music Composition Language (Page C) or Keyboard Sequencer (Page 9). This connector serves as both an input and ouput.

Connector type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 Sync Input. Pulses or tone of 1 to 20 volts P-P. Waveform unimportant. Frequency range 2 Hz to 5 kHz. Impedance 10 K ohms.

Pin 3 Click Output. Periodic pulse, rate controlled by Page 9 Sequencer or M.C.L. (Page C). Waveform is a spike of approx. 5 volts peak, approx. 5 mS wide, alternately positive and negative going.

4.14 Filter Output

Output of the bandpass filter used by the Analogue to Digital converter. It is designed to enable the operator to monitor the effect of various bandpass filter settings.

Connector type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 GROUND

Pin 3 OUTPUT. Amplitude for full-scale conversion is 10 volts P-P. Source impedance 600 ohms.

4.15 Mic In

Balanced, 600 ohms input suitable for high output dynamic or condenser microphones. When the MIC/LINE switch is in the MIC position, this input is fed to the Analogue to Digital converter.

Connector Type: Cannon 3-pin

Pin 1 GROUND

Pin 2 INPUT A

Pin 3 INPUT B

4.16 Line In

Balanced, 600 ohm line level input. This input is connected to the Analogue to Digital converter when the MIC/LINE switch is in the LINE position.

Connector Type: Cannon 3-pin

Pin 1 GROUND

Pin 2 INPUT A. Amplitude of 1.4 volts P-P required for full scale conversion.

Pin 3 INPUT B. Amplitude of 1.4 volts P-P required for full scale conversion.

4.17 ADC DIRECT

Direct input to the Analogue to Digital converter when the ADC DIRECT/ MIC LINE switch is in the ADC DIRECT position. Because this input is Direct Coupled, any D.C. offset on this input will result in a D.C. shift of a sound sample.

Connector Type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 GROUND

Pin 3 INPUT. Amplitude for full scale conversion is 10 volts P-P.

## SECTION 5. REPAIR PROCEDURE

Having isolated the faulty sub-assembly, service personel should refer to the service manual for that item for further details.

## SECTION 6. PREVENTATIVE MAINTENANCE

Under normal conditions, the only preventative maintenance required for the C.M.I. is periodical cleaning of the mesh above the blowers in the Mainframe. Refer to the C.M.I. Mainframe Service Manual for full details.

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# CMI MAINFRAME SERVICE MANUAL

FAIRLIGHT INSTRUMENTS, JULY 1982

TABLE OF CONTENTS

## 1.0 INTRODUCTION

The C.M.I. Mainframe houses all the data processing and audio genneration hardware of the C.M.I. System, including D.C. power supplies and floppy-disk drives.

This manual is designed to help service personel locate and rectify a fault in the C.M.I. mainframe.

Note that this manual only refers to the Mainframe itself. The remainder of the C.M.I. System is covered by the following related documents:

C.M.I. SYSTEM SERVICE MANUAL
MUSIC KEYBOARD SERVICE MANUAL
ALPHANUMERIC KEYBOARD SERVICE MANUAL
GRAPHICS TERMINAL MAINTENANCE MANUAL
DISK DRIVE MAINTENANCE MANUAL

### 1.1 Card Cage

A 21-slot card cage houses a printed-circuit motherboard carrying edge connectors into which the C.M.I. circuit boards are inserted. The cards can be accessed by hinging down the front panel, and they can removed from the front of the unit without requiring the use of any tools.

### 1.2 Audio Board

Cables from the front of each channel card connect to the audio board located inside the rear panel of the mainframe. This card supports a variety of audio functions, including balanced line drivers for the eight channels and mixed output.

This card is accessed by removing the four mounting screws securing the rear panel and swinging the panel down. The card itself is held in place by screws. All connections are made by plug-in cables.

### 1.3 Power Supply

D.C. power is provided by a conventional transformer/rectifier system mounted inside the left-hand end of the card cage. This supplies power for the card cage, audio board, floppy-disk drives, music keyboard and alpha-numeric keyboard.

### 1.4 Floppy-Disk Drives

Two eight-inch, double sided, single density disk drives are mounted to the right of the card cage. They connect to the power supply via a wiring harness and to the floppy-disk controller card in the card cage via a 50-way ribbon cable.

1.5 External Connections

All external connections are made by means of plug-in cables. The mainframe is normally connected to A.C. mains, Graphics Terminal Music Keyboard and audio equipment such as monitor speaker or mixing console.

The precise function of each external connection is described under Signal Lists (below).

## 2.0 SYSTEM OVERVIEW

### 2.1 General Principles
(Refer to Figure 1)

The C.M.I. is a complex special-purpose computer system which embraces many different hardware and software technologies. All processing and sound generation functions are performed by the Mainframe, while the Graphics Terminal and Keyboards serve as peripherals for operator interfacing.

The mainframe is capable of operating quite autonomously, that is, it is not reliant on any external connections for proper funtioning. Under certain conditions it is possible for a fault condition to inhibit proper Mainframe operation, so the serviceman should be aware of being misled. Of course, without the peripherals connected it is often hard to know if the system is functioning properly, but this point should be borne in mind when troubleshooting.

Operator input to the Mainframe comes from three sources: music keyboard, alpha-numeric keyboard, and lightpen. Output devices include the Graphics Display terminal, and the audio outputs. A printer may also be optionally used.

The heart of the system is the Central Processor Module, which uses two Motorola 6800 microprocessors in a dual-processor configuration. Both processors share a common buss which allows them both to communicate with the other cards in the Mainframe.

The Processor Control Module provides EPROM for system startup and bootstrap, RS-232 serial input from the keyboard, serial output to the keyboard and printer, and various other C.P.U. support functions such as interrupt prioritisation.

Main programme memory is the 64 kilobyte RAM card. This holds all the operational software, much of which is overlayed from disk as the code far excedes 64 K.

The floppy-disk controller uses Direct Memory Access techniques to transfer data between memory and the two flopp-disk drives.

The Graphics Display is a bit-mapped image of 16 kilobytes of VRAM. The Graphics Controller module displays this RAM as an array of 256 by 512 points. Special hardware on this card provides support functions for automatic vector drawing, which considerably enhances the speed of displaying graphical information.

The Lightpen Controller module interfaces the Hit and Touch signal from the Lightpen (part of the graphics display terminal) to th system buss.

Eight identical Voice Modules also share the bus. They each have 1 kilobytes of waveform RAM, as well as all the control and audi circuits required to support it.

A Voice Master module controls the voice modules, as well as providir the Analogue to Digital converter function of the system.
Audio from the Voice Modules is buffered by the Audio Output Module which provides indepenant balanced outputs for each channel as well a a mixed output.

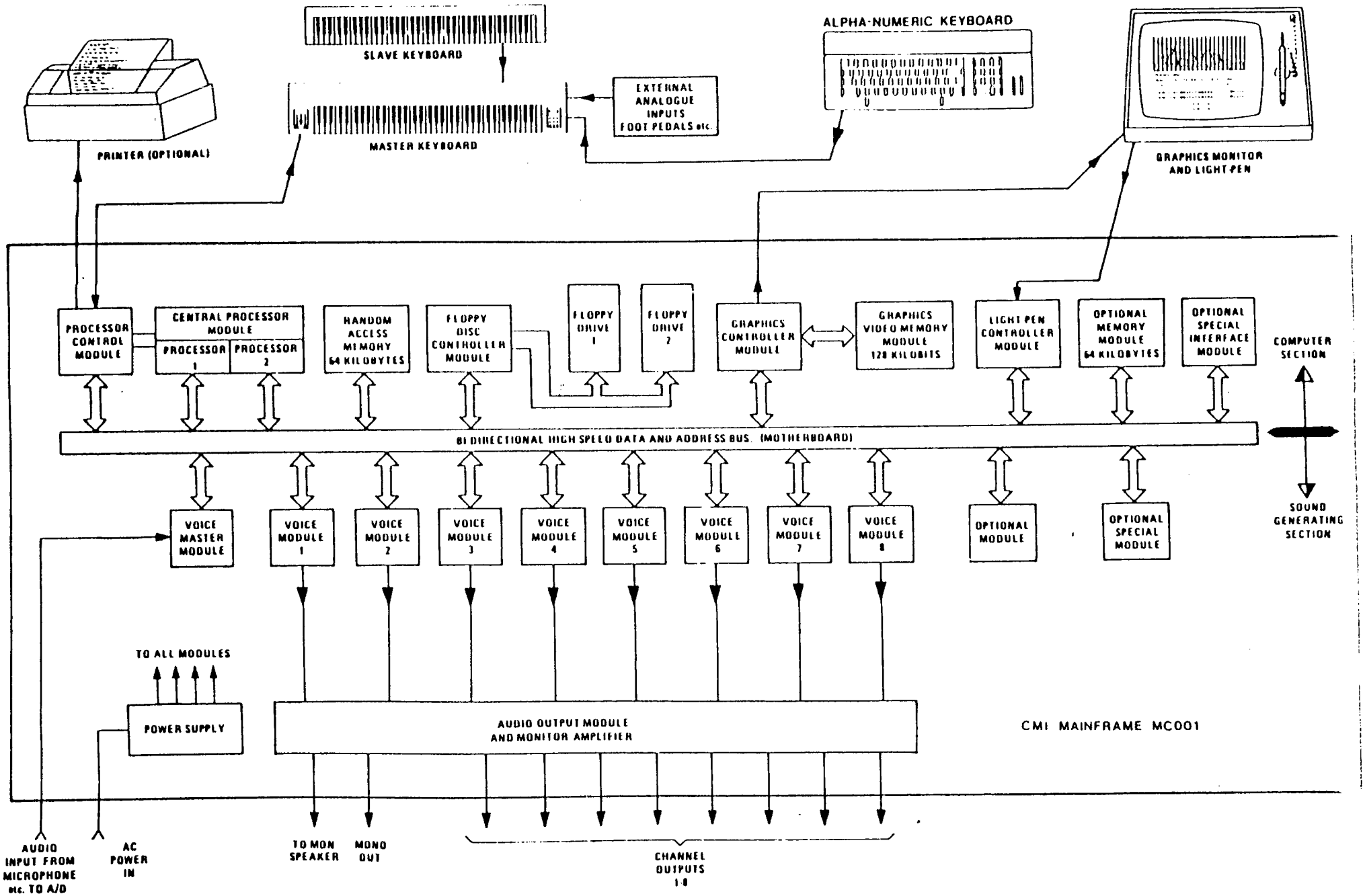



Figure 1. C.M.I. SYSTEM BLOCK DIAGRAM

## 2.2 Hardware/Software Relationships

This section gives a summary of the operational concepts involved i each of the C.M.I.'s major functions. This information should hel relate a particular software function to the appropriate piece o hardware.

The software system is divided into two main sections, the reside software and overlays. The resident part is responsible for all th real-time functions such as sound generation, keyboard inpu processing and lightpen operation. The overlays are used for th various control and sound manipulation functions provided by th display pages. Changing pages on the C.M.I. loads a new overlay fo that page from disk. Some pages use further overlays themselves, s that when certain functions are invoked from a particular page for th first time, a disk access will be made as the overlay is loaded.

Both processors have access to the 64 kilobytes of program R.A.M., s that some of the code may be executed by each processor individually and both processors can share common data structures. As a rule processor 1 is responsible for controlling the voice modules (channe cards) and handling data from the keyboard. Processor 2 carries ou the non-realtime functions such as disk I/O and graphics display.

A broad description of a range of specific functions follows.

### 2.2.1 System Startup/Boot

When power is first applied to the system, a power-on reset signal i generated for about a half second by a timer located on the Processo Control card, Q032. At the end of this time, both processors fetc restart vectors from EPROMS, also on the Q032 card and start executin the startup procedure in EPROM. Processor 1 initialises all th registers of the peripheral controller devices such as P.I.A.s an A.C.I.A.s. Processor 2 initialises the Graphics Display, clears th screen, and displays the "C.M.I. READY" message. The same message i sent to the music keyboard display via the serial link on the Q03 card. Processor 1 then loops waiting to be triggered by processor 2 which in turn loops waiting for a disk to be inserted in drive 0, a indicated by the appropriate status bit from the floppy-dis controller card QFC2.

When the sysytem disk has been correctly inserted, processor executes the first stage of the bootstrap loader firmware (located o the Q032 card). This involves reading in the boot block, which is special sector on the system disk. The code stored in the boot bloc is then executed, which completes the boot load by loading th operating system and the Page 1 overlay. When Page 1 starts up, th message Page 1 ready is sent to the music keyboard display.

### 2.2.2 Disk Operations

The C.M.I. uses two eight-inch double-sided disk drives. Format i soft sectored, 128 bytes per sector. Single density FM recording i used for extra reliability.

The drives themselves are controlled by a Western Digital FD1771 L.S.I. controller located on the Floppy Disk Controller Card QFC2.

The disk driver EPROM located on the Q032 card is used as the lowest level disk driver. Routines in this EPROM provide utilities including read sector, write sector, and verify C.R.C. which are called by the RAM-resident disk-operating system.

In the event of a disk error being detected during a read or write operation, the software will perform a number of retries, including head relocation, to try to recover from the error. If the error persists, a DISK READ/WRITE error message is displayed.

2.2.3 Graphics Display/Lightpen

The graphics display is generated by writing a bit-mapped image to the dedicated 16 kilobyte VRAM. This block of RAM is mapped in and out of the processor memory space under software control. The register for this purpose resides on the Master Card CMIØ2 (see functional description below).

The lightpen is interfaced via the Q148 Lightpen Interface card, and an interrupt to Processor 2 is generated each time the light pen Touch and Hit signals are asserted simultaneously. The processor 2 resident code is then executed to poll the lightpen co-ordinate registers and the appropriate action ensues.

The lightpen cursor is a hardware function (see Q148 functional description below).

2.2.4 Command Entry

Data arriving from the Music Keybcard is fed to the A.C.I.A. on the Q032 Processor Control Card. The A.C.I.A. generates an interrupt on processor 1 for as each byte is assembled. Data from the music keyboard and characters from the alphanumeric keyboard both arrive at the same A.C.I.A. They are distinguished by the fact that music keyboard data has the high bit set. Data from the Music Kekboard arrives in the form of three-byte packets. These are assembled and queued by processor 1 for playing. Alphanumeric characters are passed on to processor 2. This is done via common memory and an inter processor interrupt. Interprocessor interrupts are generated by special hardware located on the Master Card CMIØ2 (see functional description below).

2.2.5 Loading/Saving Sounds

Sounds are stored as contiguous "Voice" files on disk. Each voice file occupies about 2Ø kilobytes of disk space. An entry in the director on track zero gives the physical sector number of the start of the file. When a file is loaded, the directory is searched and the address of the file found. The sound is then loaded one sector at a time. Since processor 2 performs all disk operations and processor 1 controls the channel cards, data is passed between the processors via a buffer in common memory.

If more than one channel is being loaded with the same sound, multipl channels are enabled by the Master Card so that they can be written t simultaneously. See Master Card Functional Description (below) fo full details.

Saving sounds operates by the reverse process.

2.2.6 Sound Sampling

Audio input for sampling is fed to either the line input or mic inpu connector on the rear panel. It is amplified on the Audio Card CMIØ and then fed to the Master Card CMIØ2 via a 1Ø-way ribbon cable. Th signal is then attenuated by a digitally controlled attenuator an filtered by seperate low pass and high pass filters on the Audio Card These filters are also software controllable. The attenuator i controlled by the Level control on Page 8 of the CMI system software and filter cutoff points are controlled by the Filter High and Filte Low controls.

From the filters the audio is fed to the Analogue to Digita converter. The sample rate is governed by the frequency of a puls stream coming from the Channel Card in channel one position. Th sample rate is therefor established by software which sets up channe one to operate at the frequency specified as sample rate on Page 8.

Processor one is used to read data from the A-D converter and store i in the desired channel cards' waveform R.A.M. To synchronise th processor with the converter, processor one is forced to a Halt stat while a conversion is in progress, and as soon as the conversion i complete and data is ready to be read, the processor is un-halted an it reads the data. This causes Processor one's Halt L.E.D. to glo while conversions are in progress.

The Trigger Level function on Page 8 is purely a software function When the Sample command is issued, the processor starts conversion and loops until the data read is of a greater absolute value than th number specified as trigger level. It then begins transferring data t the Waveform R.A.M.

2.2.7 Music Playing

Data arriving from the music keyboard is seperated from alphanumeri keyboard strokes and assembled into three byte packets by Processor (see 2.2.4 above). The A.C.I.A. routine is interrupt driven. Once three-byte music keystroke packet has been assembled, the require note is played or stopped. The packet gives the keyboard number whether the stroke was a depression or a release, and a key velocit number.

Once the correct channel or group of channels has been identified b software relating to the keyboard/register map on Page 3, they ar started by the appropriate sequence of software commands. The channe cards generate a number of interrupts as the sound progresses an various paarmeters need to be updated.

Parameters fed to the channel card specify the pitch of the channel instantaneous amplitude, amplitude change (automatic ramping up o down), and position within the waveform.

The audio out put from each channel card is fed to the audio card by a 10-way ribbon cable plugged into the front of the card.

2.2.8 Music Keyboard Functions

As well as sending music key depression/release data to the mainframe, the music keyboard has a number of ancillary functions.

A multiplexed analogue to digital converter samples the level of the three faders on the left-hand end of the keyboard as well as the three pedal inputs on the rear. Whenever one of these changes its level by more than a certain amount, a packet of data is transmitted to the mainframe, giving the device number and the new level.

The two switches on the left of the keyboard and the three switches which plug into the rear of the keyboard are also scanned, and when any of these are opened or closed, suitable data is sent to the Mainframe.

Pressing a key on the numeric keypad on the right end of the keyboard sends a character to the Mainframe in exactly the same way as an alphanumeric key depression.

The alhphanumeric L.E.D. display on the music keyboard is driven by the serial link coming from the Mainframe. The processor in the keyboard controls the displaying of individual characters as well as backspace and clear. When messages longer than the 12 digits of the display are required, a horizontal scrolling routing in the C.M.I. system software is used.

2.2.9 Sequencer

When recording on the Sequencer (Page 9), a hardware timer located on the Master Card CMI02 is used to measure the elapsed time between events such as key depressions or releases. As each event takes place procesor 1 assembles the keystroke or control change data into a five byte packet along with the time to the next event and queues it. When the queue is half full, Processor 2 writes the data to the sequence file on disk, emptying the queue.

In playback mode, Processor 2 reads the playback file into a queue Processor 1 takes keystroke and timing packets from the queue and set the timer on the Master Card for the time to the next event. When this time has elapsed, the timer generates an interrupt and the next event is pulled from the queue and played.

The Merge function uses both Record and Playback processes simultaneously.

When running on Internal Synch, the timer operates by counting the system clock. When External Synch is specified, the timer configured to use the external clock, which is derived from the Sync input on the rear of the Mainframe, via suitable signal processing circuitry. The external synch is fed through another programmable timer so that it can be divided if desired.

2.2.10 Music Composition Language

M.C.L. data is store on disk in the form of M.C.L. notation. The Lo
command simply causes processor 2 to read the file specified in
R.A.M. No processing of the data is done at this stage.

When the Play command is issued, Processor 2 starts compiling t
source code and generates keystroke packets which it queues along wi
the time to the next event, which it calculates from the combinati
of up to eight parts which it may be playing simultaneously. The
packets are then processed by processor 1 in much the same way as f
the Sequencer (described above).

Internal/External synchronisation works the same way as for t
Sequencer.

## 3.0 SPECIFICATIONS

### 3.1 ELECTRICAL

Power Requirements
  Mains Voltage: 100-120 or 200-250 switch selectable
  Mains Current: 2 amps @ 240 V, 4 amps @ 120 V
  Mains Frequency: 50/60 Hz

### 3.2 AUDIO

Channel Outputs
  Connector type: Cannon XLR 3 pin (Balanced)
  Number of Channels: 8 (maximum)
  Output Level: 3.7 volts p-p
  Output impedance: 600 ohms
  Output load: Must be greater than 600 ohms

Mixed Line Output
  Same as Channel outputs

Monitor Speaker Output
  Connector type: Cannon XLR 3 pin
  Load impedance: 4 ohms (minimum)
  Power output at clipping: 20 watts max.
    (This output is not intended to be driven to full outp
    continuously.)

Headphone output
  Connector type: 1/4" Stereo Phones
  Signal: Derived from monitor speaker output via 100 ohm resistor

Synch Input
  Connector type: Cannon XLR 3 pin
  Level: 1 volt (min) 20 volt (max) p-p.
  Frequency range: 2 Hz - 5 KHz
  Impedance: 10KHz

Click Output
  Connector Type: Cannon XLR 3 pin
  Output signal: 5 volt spike, approx 5 mS wide, alternative
  negative and positive going.

Mic Input
  Connector type: Cannon XLR 3 pin
  Impedance: 6000
  Microphone type: Balanced, high output dynamic or condenser type

Line Input
  Connector type: Cannon XLR 3 pin
  Input signal: Balanced
  Sensitivity: 1.4 volts p-p required for full scale conversion.
  Impedance 600 ohms.

ADC Direct Input

Connector Type: Cannon XLR 3 pin
Input Signal: D.C. coupled
Sensitivity: 10 volts p-p for full-scale conversion
Impedance: 100 K ohms

3.3 DIGITAL

Processor: Dual M6800

Memory: 64 kilobytes Programme RAM
16 kilobytes Video RAM
128 kilobytes Waveform RAM

Floppy Disk: 2x YE DATA YD174
8 inch double sided, single density
Soft sectored, 128 bytes per sector

Graphics Display: Bit mapped VRAM
Composite video output
1 volt p-p nominal
75 ohms impedance

Input/Output: Serial RS232-C, 9600 Baud

3.4 MECHANICAL

Dimensions: Width: 750 mm
Depth: 450 mm
Height: 320 mm

Weight: 40 kilograms

## 4.0 FUNCTIONAL DESCRIPTION

This section describes the operation of each of the circuit boar used in the C.M.I. mainframe. The information is presented primari to give service personel a thorough understanding of the operation the system as an aid to fault diagnosis to the board level. Once t faulty board has been identified, it is recomended that the Mainfra be repaired by board exchange. The faulty item should be returned Fairlight Instruments for repair.

## @CC4.1 Q-026 DUAL 6800 CENTRAL PROCESSOR FUNCTIONAL DESCRIPTION

### 4.1.1 INTRODUCTION

The Dual processor card operates each processor into a commcn addre and data bus in an interleaved manner, each processor therefore m simultaneously access the same memory location without any contenti problems.

This unique manner of operation allows for full "synergisti operation, and either synchronous or asynchronous relationshi between processors.

The memory addresses are issued to the bus 225 nanoseconds prior the access cycle, allowing addresses to be modified by an extern memory mapping unit card for applications requiring in excess of 6 bytes of memory space. Many global timing signals are issued from t processor, these signals greatly reduce the complexity of many of t other cards in the system.

### 4.1.2 TIMING & MEMORY CONTROL LOGIC
(Refer to drawing Q026-01)

#### 4.1.2.1 Master Timing Signals

All system timing signals are derived from crystal-controlled 40M oscillator Q5. Flip-flop E3 divides this pulse train by two to provi a symmetrical 20 MHz square wave, which is made available as a timi signal on the bus via E7 on edge connector pin 43. Quad D-type lat F2, together with one quarter of quad flip-flop E1, are configured a twisted-tail ring counter which generates 10 unique states each 50 nanoseconds duration. The required states are decoded by NAND gat F1 and AND gates F3.

#### 4.1.2.2 Dynamic Memory Timing Signals

Four non-inverting buffers of D1 are driven by latch E1 to provide C (Column Address Strobe), RAS (Row Address Strobe), CA (Column Addre (asserted low) and RA (Row Address, asserted low). RAS is delay relative to CAS by about 20 nS by the propagation delay of A7. RA a CA are complimentary signals.

4.1.2.3 Data and Address Buss Multiplexing

Flip-flops F4 and F5, along with associated gating, generate th processor drive signals D1, D1, D2 D2 from which the phase 1 and phas 2 clocks for each processor are derived (see next section). The syste address bus is multiplexed by the ADDRESS signals ADD(1) and ADD(2) One-of-four decoders F8 and F9 are used to enable the approprit address and data buffers to the bus to perform the multiplexing. Th data buffer enable signals WRITE1, WRITE2, READ1, READ2 are generate by logical combinations of Phase 2, VMA and Read/Write, performed b F8. The address buss is actually multiplexed four ways, as th vectored interrupt system may also acquire the buss for eithe processor's cycle. The address buffer enables are a function of th Address signal and the Interrupt acknowledge, performed by E4.

Phase 2 reference and Address references for each Processor are fed t the bus via bus drivers.

4.1.2.4 Interrupt Strobe Generation

Dual D-type flip-flop A8 and 3-input AND gate A7 feed Interrupt Latc Strobe pulses to the buss. These are used by the Priority Interrup Control Units (PICUs) used to provide Vectored Interrupts, and also t strobe the vector address latches E6 and E( on sheet 3. The PICUs ar located elsewhere in the system. These signals strobe the priorit latches continuously, until and interrupt is acknowledged. In this wa the Interrupt Priority is maintained at its latest level regardless c delay between an interrupt request being received by the PICU and th associated vector-fetch cycle being executed.

4.1.2.5 Direct Memory Access

DMA requests for each processor are clocked into flip-flop D6 on th falling edge of phase two signals of the respective processors. Dl acknowledgement is sent to the buss via buffers and the drive signa to the processors are suspended in the phase 1 state for the durati of the DMA cycle. The maximum permissable DMA duration is microseconds. Worst-case DMA latency is 1 microsecond.

4.1.3 CLOCK DRIVERS, CPUs and VECTOR-FETCH DECODERS
(Refer to drawing Q026-02)

4.1.3.1 Processor Clocks

Non-overlapping clocks for processor Phase 1 and Phase 2 signals a generated from drive signals D1 and D2. Emitter followers Q1-Q4 a provided to ensure legitimate MOS logic levels as required by the 68 (<.5 volts low, > 4.5 volts high). Cross-coupling between phase 1 a phase 2 drivers ensures that each phase stays low until after t other phase has gone low.

4.1.3.2 Vector-Fetch Decoders

A series of open-collector AND gates follow the processor address bu state to detect addresses in the range FFF8-FFFF. The correspond the processor fetching vectors for IRQ, SWI, NMI and RESTART.

Restart vectors come from ROM so when this is sensed the ROM must b enabled and the RAM disabled. This is achieved by the ROMEN (RO ENABLE) signal on Buss pin 44. On detection of an FFFE-FFFF addres (restart being fetched), the one-of-four decoder B8 generates a appropriate signal, and both processors ROMEN is multiplexed onto th bus by OR gate C8.

On detection of and Interrupt Request vector address from th processor, an INT signal is generated by one-of-four decoder B8, whic causes the normal address buss drivers for bits 1 to 4 to be disable and the Interrupt Address buffers (on shhet 3) to be enabled in lieu.

4.1.4 BUSS DRIVERS & INTERUPT LEVEL MULTIPLEXER
(Refer to drawing Q026-3)

4.1.4.1 Address Buffers/Multiplexers

Two sets of tri-state buffers are alternately enabled to provid address buss multiplexing. ADD1 and ADD2 enableprocessor 1 an processor two addresses to the buss alternately, except during a DM cycle, in which case the buss is tri-state. Bits 1 to 4 of the addres buss are multiplexed between normal processor addresses and addresse coming from the Interrupt Prioritizer, depending on the signals NAD and IADI. When an IPQ vector fetch is attempted, the buffers D3 and D are enabled instead of the normal address buffers, so that th interrupt priority which has been latched by flip-flops E6 or E become Bits 1 to 4 of the address from which the vector will b fetched. The vector fetch is a double-byte, so address bit Ø is lef un-multiplexed.

4.1.4.2 Data Buffers/Multiplexers

Inverting tri-state buffers D2, E2, D5, E5 are used to multiple Processor 1 and Processor 2 data. Data is received when READ is lo and transmitted when WRITE is high.

## 4.2 C032 C.P.U. CONTROL CARD FUNCTIONAL DESCRIPTION

### 4.2.1 INTRODUCTION

The CPU Control Card provides several support functions required
the CPU card. These include startup and bootstrap ROM, seri
communications, interrupt prioritisation and a parallel port.

#### 4.2.1.1 Addressing Map

This card occupies the last 4K bytes of the 65K byte phsyical memo
addressing space and is set up as follows:-

| ADDRESS (HEX) | FUNCTION |
|---|---|
| F000-F3FF | Common ROM |
| F400-F7FF | Common ROM |
| F800-FBFF | 2 unique ROMs, one for each processor |
| FC00-FCEF unused | Available for user peripherals |
| FCF0 | Serial I/O control |
| FCF4,FCF5 | ACIA registers |
| FCF8-FCFB | PIA registers |
| FCFC | CPU#1 interrupt prioritiser |
| FCFD | CPU#2 interrupt prioritiser |
| FD00-FEFF | Shared 512 byte RAM |
| FF00-FFFF | Unique 256 byte RAM for each processor |

#### 4.2.1.2 Restart and Interrupt Vectors

RAM space allocated uniquely to each processor provide independe
restart and interrupt vectoring. The vector locations are as follow

| ADDRESS (HEX) | VECTOR (6800 SYSTEM) | VECTOR (6809 SYSTEM) |
|---|---|---|
| FFFE/F | Restart | Restart |
| FFFC/D | NMI | NMI |
| FFFA/B | SWI | SWI1 |
| FFF8/9 | Unused | Unused |
| FFF6/7 | Unused | FIRQ |
| FFF4/5 | Unused | SWI2 |
| FFF2/3 | Unused | SWI3 |
| FFF0/1 | Unused | Unused |
| FFEE/F | IRQ level 7 (lowest) | IRQ level 7 |
| FFEC/D | IRQ level 6 | IRQ level 6 |
| FFEA/B | IRQ level 5 | IRQ level 5 |
| FFE8/9 | IRQ level 4 | IRQ level 4 |
| FFE6/7 | IRQ level 3 | IRQ level 3 |
| FFE4/5 | IRQ level 2 | IRQ level 2 |
| FFE2/3 | IRQ level 1 | IRQ level 1 |
| FFE0/1 | IRQ level 0 (highest) | IRQ level 0 (highest) |
| FFDE/F | Monitor workspace | IRQ level 15 (lowest) |
| FFDC/D | Monitor workspace | IRQ level 14 |
| FFDA/B | Monitor workspace | IRQ level 13 |
| FFD8/9 | Monitor workspace | IRQ level 12 |
| FFD6/7 | Monitor workspace | IRQ level 11 |
| FFD4/5 | Monitor workspace | IRQ level 10 |
| FFD2/3 | Monitor workspace | IRQ level 9 |
| FFD0/1 | Monitor workspace | IRQ level 8 |

4.16 Line In

Balanced, 600 ohm line level input. This input is connected to the Analogue to Digital converter when the MIC/LINE switch is in the LINE position.

Connector Type: Cannon 3-pin

Pin 1 GROUND

Pin 2 INPUT A. Amplitude of 1.4 volts P-P required for full scale conversion.

Pin 3 INPUT B. Amplitude of 1.4 volts P-P required for full scale conversion.

4.17 ADC DIRECT

Direct input to the Analogue to Digital converter when the ADC DIRECT/ MIC LINE switch is in the ADC DIRECT position. Because this input is Direct Coupled, any D.C. offset on this input will result in a D.C. shift of a sound sample.

Connector Type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 GROUND

Pin 3 INPUT. Amplitude for full scale conversion is 10 volts P-P.

4.2.1.4 System Bootstrap/ Disk Controller Firmware

This EPROM is used by Processor 2 for disk operations and occupies locations F800 to FBFF in the unique ROM space for CPU#2. The following functions are provided:-

* Boot load operating system from disc
* Initialise disc controller
* Read full last sector
* Read partial last sector
* Read verify (CRC check only)
* Write and verify CRC
* Restore head (seek track 0)
* Seek to specified track
* Write test
* Write D.D. mark to sector
* Write sectors and verify CRC
* Write sectors and don't verify CRC
* Check and abort if non recoverable error

4.2.2 ADDRESS DECODING AND RAM REFRESH CONTROL
(Refer to drawing Q032-01)

4.2.2.1 Address Decoding

The System Data Buss is buffered by non-inverting buffers A1 and A NAND gate A2 generates an output (asserted LOW) when an address in th range FXXX is detected. This is fed out to the buss on edge connecto pin 65B (RAMINH) to disable RAM when accesses to this address rang are made. Further decoding by one-of-four selectors B1 generate selec signals for the four EPROMS, ROM1 through ROM4. ROM1 and ROM2 are the processor-unique ROMs, which are selected by the ADD1 and ADD (address) signals from the buss, which are gated in by NAND gates B6.

Selection of the on-card static RAM and peripheral devices in the FCFX range are also decoded.

These six select signals are latched by hex flip-flop B7. Hex flip-flops B2 and B3 latch the 10 low-order address bits, as well as the READ/WRITE and Card Select signals.

4.2.2.2 RAM Refresh Control

Rate multiplier B8 is configured to produce a 1 microsecond pulse every 16 microseconds. This output (HLTST) generates a DMA request for Processor 1 (REQ1). When this request is acknowledged, by the ACK1 buss signal (asserted HIGH), NAND gate A7 generates a REF (Refresh, asserted LOW) signal on the buss, which signals a refresh cycle to the dynamic RAMs in the system. At the same time, the output of the refresh address counter A5 is driven onto the buss by tri-state buffers A4. At the completion of the refresh (DMA) cycle, the refresh address counter is incremented ready for the next cycle.

4.2.3 EPROM, RAM, ACIA, PIA
(Refer to drawing Q032-02)

4.2.3.1 Static RAM

A small amount of static RAM is provided for use as scratchpad durin disk calls and monitor firmware execution. It is organised as follows

| | |
|---|---|
| CPU #1 | FF00-FFFD |
| CPU #2 | FF00-FFFD |
| Both | FD00-FEFF |

The addressing function for this purpose is generated by multiplexe C8 which is driven by an OR funtion of address bits 8 and 9. The RA itself is in the form of two 1k X 4 devices.

4.2.3.2 EPROM

Four kilobytes of U.V. erasable ROM are used. These are 2708 type.

Their functions are:

| Location | Address Range | CPU # | Function |
|---|---|---|---|
| D2 | F800-FBFF | 1 | Startup and clock |
| D4 | F800-FBFF | 2 | Disk boot and controller |
| D5 | F400-F7FF | Both | I/O functions |
| D6 | F000-F3FF | Both | Debug monitor |

4.2.3.3 ACIA (Asynchronous Communications Interface Adapter)

A 6850 ACIA (E8) is used to receive and transmit serial data. The BAU rate is determined by seperate Receive and Transmit Clock siganls coming from the baud-rate generator on the front panel card (0036) vi the 26-way ribbon cable on the front edge of the Q032 card.

Interrupts generated by the ACIA go to the system buss via pin 68B o the edge connector.

Data input and output level conversion for the RS232 standard i provided by circuitry on Sheet 3.

4.2.3.4 PIA (Peripheral Interface Adapter)

A PIA (F8,9) is used to provide two general purpose parallel ports Peripheral connections are made through a 26-way ribbon cabl connector on the front of the card.

Interrupts from the PIA are presented to the bus via pins 66B and 67B

The PIA is also used by processor 1 to provide a real-time cloc function via its CB1 input which is clocked continuously by RTC pulses coming from the refresh address counter A5 on sheet 1.

## 4.2.4 TERMINAL INTERFACE, MANUAL CONTROLS, POWER-ON RESET

### 4.2.4.1 Terminal Interface

RS232 receivers and drivers are provided to interface the ACIA to serial data to and from peripheral devices. F1 is the RS232 driver. Two data output paths are provided, called DATAØ and DATA1. Device control signals DONØ and DON1 are used to enable external peripherals. The serial-I/O control latch D1 is used to select which of the data paths is enabled, and which devices are switched on. It is configured by writing to FCFØ. As well as selecting data output paths, bits 2 and 3 of this latch select which of two "busy" flags are enabled to the CTS pin of the ACIA.

Bit 4 of the Serial I/O control is used to select the polarity of the busy flag by maens of exclusive-or gate E1.

Bit 5 is used to control the threshold of the busy flag bits of RS232 receiver F2. When bit 5 is HIGH, transistor Q1 is held off, and a negative bias is applied. With bit 5 LOW, Q1 turns on and biases the receivers positively.

The opto-isolator is not normally used, but its outputs are available at the edge connector if required. It is turned on by writing Ø1 to the two high bits of the serial I/O control latch.

### 4.2.4.2. Manual Controls

Restart and interrupt contols are provided on the front-panel card Q036. The push-button switches are debounced by R/S flip-flops made up by gates in F3. Processor selection is aceived by NAND gates F6, which also drive the buss.

Processor Halt controls are latched by flip-flops F5. This debounces the switches and also ensures that the 6800 timing requirements for HALT control are met.

When a WAIT state has been achieved, the Buss Available signals from the CPU card W1 and W2 drive open-collector buffers E5 to turn on the WAIT LEDs on the front panel.

### 4.2.4.3 Power-on Reset

555 Timer E3 is used to generate a system reset signal on power-up. This is a low-going pulse of about 500 milliseconds on buss pin 42.

### 4.2.5 INTERRUPT PRIORITY LOGIC AND DATA BUFFERS
(Refer to drawing Q032-04)

#### 4.2.5.1 Interrupt Priority Logic

8214 Priority Interrupt Control Units (PICU) are used to lat
interrupt requests and generate a priority level which is used by t
CPU card to create an interrupt vector address.

The priority level for each PICU is established by writing t
compliment of the desired priority level into the status rtegiste
The address for CPU 1 is FCFD, for CPU 2 it is FCFC. Decoding for thi
purpose is performed by one-of-eight selector E10.

Interrupt requests generated by the PICU are latched by flip-flo
D10, which are reset when the PICUs are written to to establish t
new pricrity level mask.

The PICUs are clocked by Interrupt Latch Strobe signals from the bu
(ILS1 and ILS2).

Each PICU supports up to eight levels of interrupt. To expand t
beycnd eight, the PICUs can be daisy-chained by changing links o
terminal strip T1.

#### 4.2.5.2 Data Buffers

Inverting tri-state buffers B4 and B5 interface the local data buss t
the system data buss. The direction of data transfer is controlled b
PEAD.

## 4.3 Q-996 64K MAPPING RAM CARD FUNCTIONAL DESCRIPTION

### 4.3.1 INTRODUCTION

The 64K RAM Card contains 32 x 16K x 1 bit dynamic RAM chips. The RAM runs at a cycle time of 500 nS and is refreshed by a global refresh system contained on the Processor Control Card.

In addition to the dynamic RAM, a fast 16 x 4 bit static RAM is used to provide an independent mapping of each of four 16K logical processor spaces to the 64K physical address space. This mapping RAM is also responsible for enabling the entire card when more than one 64K RAM card is installed in the system. A four-bit module select switch is used for this purpose.

### 4.3.2 ADDRESS DECODING & MAPPING LOGIC
(Refer to drawing Q996-01)

#### 4.3.2.1 Address Decoding

The mapping register base occupies memory space from FC40 to FC4F. Accesses to these addresses are decoded by NAND gate C2, and latched by D-type flip-flop B1. The low four bits of the address are also latched by B1 and these are selected by 4-bit multiplexer B2 when writing to FC4X.

#### 4.3.2.2 Mapping Logic

The mapping register B3 is a high-speed RAM of 16 words of 4 bits. When writing to the mapping register, the four high data bits are compared to the module number set up on the Module Select D.I.L. switch, and if it matches, a 1 is written to data bit 3. This bit is used as the card enable bit when subsequent accesses are made to the RAM. Bit zero is a 0 for write protect, bits 1 and 2 select which of the four 16k blocks is enabled.

When accesses are made to the main RAM, the high two bits of the address along with the address1/address2 multiplex signal and the mapA/mapB select signal form the address to the mapping register. Data bits 0 and 1 from the mapping register select one-of-four blocks via selector D2, which is enabled by a logic zero on bit 3. The block select bits, card select and Read/Write are latched by flip-flop D1.

The card select, read/write and Column Address (BCA) are ANDed by E1 to produce the READ enable for the data buffers (on sheet 2). The read/write signal is buffered by inverters F1 and drive the read/write busses for the RAM array via series termination resistors.

The four block select signals are used to gate the Column Address Strobes (CAS) and Row Address Strobes (RAS) which drive the RAM array via buffer E3. During Refresh cycles, all four RAS signals are enabled by gates E2, enabled by the latched refresh signal (LREF) from flip-flop B1.

## 4.4 QFC2_FLOPPY_DISK_CONTROLLER_FUNCTIONAL_DESCRIPTION

### 4.4.1 INTRODUCTION

The Floppy Disc Controller/Formatter uses a Western Digital FD1771 controller LSI. It is designed to work with CPU #2, transferring data to and from memory by DMA on Processor 2. Once a data transfer is set up the processor may continue processing other tasks until the interrupt for "command done" is issued by the controller.

#### 4.4.1.1 Address Map

| ADDRESS (HEX) | READ | WRITE |
|---|---|---|
| FCE0 | status read | command reg |
| FCE1 | track reg | track reg |
| FCE2 | sector reg | sector reg |
| FCE3 | data reg | data reg |
| FCE4/5 | - | DMA start address |
| FCE6 | - | DMA mode/drive sel |
| FCE7 | DMA status | - |

The DMA transfer byte count is inherent in the transfer type.

#### 4.4.1.2 Commands

The following commands may be issued to the command register to effect disc operations:-

* Restore head to track zero
* Seek to track
* Step in current direction
* Step in
* Step out
* Read (single/multiple)
* Write (single/multiple)
* Read address mark
* Read track (format information)
* Write track (format information)
* Force interrupt.

Various options exist within commands which specify step rate, head loading, address verification, and other actions desirable during the execution of the command.

For full details of these commands, refer to the FD1771 manufacturers data sheets.

### 4.4.2 DATA BUFFERS, DMA ADDRESS COUNTER, VERIFY COMPARATOR (Refer to drawing QFC2-01)

#### 4.4.2.1 DMA Address Counters

Sixteen bit counter chain B1 to B4 is used to provide the address for DMA transfers. The starting address for each disc transaction is established by writing the double-byte address to location $FCE4. This causes the address to be preset into the DMA address counter by means of parallel-load strobe pulses STAL (low byte) and STAH (high byte).

4.4.2.2 Data Buffers

Data is propagated from the system data bus via latches B5 and B6 which hold the data across the processor 1 phase. This latched data also become the DATA FROM BUS via buffers A7, A8 to the floppy-controller L.S.I.

Data written to the system control byte at $FCE6 is latched by hex D-type flip-flop C4. DA0, DA1 are DRIVE SELECT addressing for selecting which of four disk drives is enabled. FN0,FN1 are FUNCTION SELECTS, which choose one of RESET (00), WRITE (01), READ (10), VERIFY (11).

Bit 4 of the system control byte selects which side of the disk is being accessed when used with dual-sided disk drives. Bit 5 is an INTERRUPT ENABLE.

4.4.2.3 Verify Comparator

A special feature of the CFC2 is the ability to verify data from disk against memory without actually transferring it.

EXCLUSIVE-OR gates B7,B8 are used to compare D.M.A.derived data to data read from disk from the controller L.S.I. data CD0-7.

4.4.3 ADDRESS DECODING, CONTROLLER L.S.I., DRIVE SELECT
(Refer to drawing CFC2-01)

4.4.3.1 Address Decoding

Address range $FCEX is decoded by gates A4 and C3 and latched by C1. The clock for this latch (LSTB) is a derivative of processor two phase two, which makes the CFC2 processor two unique. The on-card buss operates at 1MHz, half the system speed.

Addresses FCE0-FCE3 are used by the FD1771. Addresses FCE4-FCE7 are used to write to the DMA address counters and funtion select latch. These are enabled by the appropriate outputs from one-of-four selector C2.

4.4.3.2 Controller L.S.I.

The -5 volt supply required by the FD1771 is derived from the -12 vol supply by a 79L05 voltage regulator I.C.

Inverting buffers D6 are used to interface the FD1771 L.S.I controller to the disc drive cable. Incoming disc status signal TR00 (track Zero), IP (Index Pulse), WPRT (write protect) and READ are pulled up by 150 ohm terminating resistors.

The Interrupt Request from the L.S.I. (INTRQ) is gated with th Interrupt Enable (IENA) to provide an open-collector interrupt signa for the system I.R.Q.

One-shot D7 is the 35ms head load timer (see FD1771 data sheet).
4.4.3.3 Drive Select

Up to four drives can be controlled by the QFC2. The two-bit drive number written to $FCE6 is decoded to individual drive slect lines by one-of-four selector D4. The interface cable is driven by buffers C5. Drive reversal switch SW1 is provided to allow inversion of the low order drive select bit. This is used mainly for swapping drives for troubleshooting purposes.

4.4.4 DMA LOGIC
(Refer to drawing QFC2-03)

Data requests from the FD1771 (DRQ) are synchronised with Processor 2 Phase 2 using flip-flops D8,D9. This sets up a D.M.A. request to the processor (RDMA). D.M.A. cycles are granted by ACK acknowledge signal (from sheet 2).

Depending on which function has been requested (Reset, Read, Write, Verify decoded by D4) the required DTB (Data to Bus), and ATB (Address to Bus) signals are issued.

Data mismatches encountered during a verify cycle are clocked through flip-flop D5 and can be read as the VERFER status bit (bit 7) of status byte $FCE7.

4.4.5 Data Seperator
(Refer to drawing QFC2-04)

The data seperator is used to generate seperate CLOCK and DATA pulses from the FM encoded READ DATA supplied by the disc drive.

The operation of the data seperator is best understood by referring to the timing diagram, drawing number QFC2-04. This shows the pulse timings representing operation after the data seperator has been locked in phase and proper recovery is in progress.

Composite read data, consisting of both CLOCK and DATA signals, arrive at pin 5 of the floppy disc cable connector. The line is terminated by a 150 ohm pull up resistor. Three gates of E3 are configured to multiplex the READ DATA to one of two paths, that is either CLK or DATA.

DATA pulses fire a 2.7 uS one shot (half E1) to produce a pulse as shown at test point TP1. The next pulse that arrives will be the following CLK pulse, which resets this one-shot and fires the second 2.7 uS one-shot. This toggles the 3 gating to allow the following DATA pulse through, if there is one.

Initial synchronisation is achieved by flip-flop chain D1,D2. This detects the occurrence of eight suspected DATA pulses in a row without any CLOCK pulses. This occurs when the seperator is out of phase and a byte of ZERO is read. This should be read as eight clock bits with no data bits, but if the seperator is not in phase it is detected as an error condition, and the one-shots are forced to reset.

## 4.5 Q045 GRAPHIC DISPLAY CONTROLLER FUNCTIONAL DESCRIPTION

### 4.5.1 INTRODUCTION

The Q045 is used in conjunction with a Q025 VRAM card to provide a graphics display system. The 16 kilobytes VRAM is displayed as an array of 512 points (horizontal) by 256 lines (vertical).

It also interfaces to the Q148 Light Pen controller.

To increase graphics drawing speed, extensive use is made of special hardware functions which provide automatic address incrementing or decrementing along either or both axes.

Locations FCD0 to FCDC perform store and auto-increment/decrement functions as follows:

| | |
|---|---|
| FCD0 | Just store at current position |
| FCD1 | Store and Inc Y |
| FCD2 | Store and Dec Y |
| FCD3 | Store as byte at current Pos |
| FCD4 | Store and Inc X |
| FCD5 | Store and Inc X, Inc Y |
| FCD6 | Store and Inc X, Dec Y |
| FCD7 | Store as byte, and Inc X |
| FCD8 | Store and Dec X |
| FCD9 | Store and Dec X, Inc Y |
| FCDA | Store and Dec X, Dec Y |
| FCDB | Store as byte and Dec X |
| FCDC | Load scroll latch |

The pattern contained in the register stores at the particular location above may be varied to produce solids or various forms of dotted or dashed lines on the screen.

The current position is established by directly accessing the VRAM with a dummy read. Subsequent use of the special locations then work from that position on the screen in various directions.
The byte mode operations are provided for the writing of alpha-numeric data to the screen. Note that byte mode operations only work in the vertical (X) direction. This direction requires the actual VRAM address to be advanced by 64 bytes. Byte mode in the (Y) horizontal direction is achieved by storing directly into successive locations in the VRAM.

All non-byte operations store one point on the screen. What is written to this point (0 or 1) depends on what is in the corresponding bit position of the accumulator used to store the data.

### 4.5.2 SYNCH GENERATOR, SEPERATOR AND REGENERATOR
(Refer to drawing Q045-01)

#### 4.5.2.1 Synch Generator

The Graphics Controller Card uses one of two alternative synch generator I.C.s. Both are at location F6 and are driven by crystal oscillator E5. Composite synch appears at S01 pin 1. This is normally

linked on the card to SO1 pin 4, in which case the card operates off internal synch.

4.5.2.2 Synch Seperator

Composite Synch or composite video from SO1 pin 4 is buffered by emitter-follower Q1 and any video information is stripped off by synch seperator Q2 and Schmitt trigger D4.

4.5.2.3. Synch Regenerator

The composite synch is fed to two one-shots, F7. Vertical synch pulses are detected by looking for pulses greater than 12 microseconds wide One half of F7 operates with a time constant of 12 microseconds, s that pulses of greater than 12 microseconds will cause a 1 to d clocked into D-type flip-flop F8.

Horizontal synch pulses are regenerated by the other half of F7, which has a time constant of 50 microseconds (just less than one line of 6 microseconds).

The Horizontal Clock pulses HCLK (one per line) are used to cloc presettable counters F9, F10, E10, D10. F9 and F10 count off line from the top of the picture to determine the vertical positioning o the active display area. Link options are provided to adjust th vertical position, and these are factory set for 25 lines. When thes 25 lines have been counted, a Terminal Count from F10 generates narrow RESET pulse from NAND gate E8.

The Terminal Count also causes a logic Ø to be presented at the Dat input of D-type flip-flop F8, which causes a logic Ø to be clocke through on the next HCLK. This generates the UNBLNK signal to disabl blanking and start the display.

Counters E10 and D10 are enabled by the UNBLNK signal and then activ display lines are counted. The counters are factory preset for 25 lines of vertical display. Once the 256 lines have been counted, th Terminal Count from D10 causes the blanking flip-flop F8 to be se again, blanking the display.

4.5.3 VIDEO GENERATION LOGIC
(Refer to drawing Q045-02)

4.5.3.1 Bit Clock Generation

Each line synch pulse HCLK triggers one-shot F4 to procuce a puls whose width is determined by the setting of RV1, the POSITION control At the end of the pulse, the active line begins by removing the M (Master Reset) condition from bit counters D1, D2 and D2,3 ar enabling AND gate E2. The bit-rate oscillator is fromed by one-shot F and associated feed-back gates. The frequency of oscillation i governed by the period of the one-shot which is adjustable by means o RV2, thw WIDTH control. The bit rate pulses from F4 are used to cloc the counter chain which counts off 256 or 512 bits per line (the car is factory set for 512). When the required count has been achieve inverter E2,3 diables AND gate E2, stopping the bit rate oscillator.

4.5.3.2 Video FIFO and Shift Register

To compensate for the fact that bytes from memory need to be fetched at greater than 1 MHz for dispalying, a FIFO register (First-in, first-out) is used. Data from the VRAM (RDØ-RD7) is latched by octal latch C7. When the FIFO input is not full, the IR signal causes a data request to by clocked through flip-flop C8, which in turn generates a Shift In (SI) pulse to the FIFO. This occurs every microsecond until the FIFO input queue is full, as indicated by IR returning to a logic zero.

Data is shifted out of the FIFO to the parallel-in serial-out shift register D6 by SO (Shift Out) pulses coming from the bit counter chain. These are derived from bit 3 of the counter, resulting in one byte being transferred from the FIFO to the shift register every eight picture bits. The shift register Parallel Load control is strobed during the first of the eight bit periods by decoder E1. The picture information is shifted out by clock pulses from the bit rate oscillator F4.

4.5.3.3. Video Output

Video data from the shift register is EXCLUSIVE-ORed with the INV (Invert) signal from edge connector pin 75. With a logic 1 at this pin the picture appears normally with set bits in the VRAM displayed as bright pixels. If a logic zero is applied, the picture is inverted (negative) so that ones in VRAM appear as black pixels on a bright background.

The output from the exclusive-or gate E3 is serrated at the bit rate by ANDING with VST (Video Strobe) pulses from E1. This is done to avoid horizontally adjacent dots merging to appear brighter than vertically adjacent ones.

The serrated video is then blanked by gating with UNBLNK to remove unwanted (inactive) display time from the display. Synch is added to the video by resistor network R37, R37, R38 and buffered for low impedance driving by transistor Q4.

Composite synch (without vidoe information) is available at pin 5 of SO1 and vidoe without synch appears at pin 9 of SC1.

4.5.4 SELECT LOGIC AND DATA CONTROL
(See drawing Q045-03)

4.5.4.1 Address Decoding

The Graphics Controller occupies two areas of memory space. The VRAM uses 16 kilobytes from $8000 to $BFFF. The various auto-incrementing portholes use 16 bytes from $FCDØ to $FCDF. Addresses in the $FCDX range are decoded by NAND gate A5. VRAM addresses in the $8000 range are decoded by NAND gate D5. Both these are enabled by ANI gate E2, which ANDs VMA (Valid Memory Address), ENBL (Enable) and BADD2X, which is used to determine which processor has access to the card.

The select signals from this gating are latched, along with the four least significant address bits, by hex D-type flip-flop B6.

The Read/Write signal from the buss is latched by one half of flip-flop C8, and gated with the latched select signals to enable the read and write buffers B7 and A7.

The 16 auto-increment functions are decoded from the four least significant address bits by dual one-of-four selector B8.

4.5.4.2 Data Buffers

Quad buss transceivers A7 and B7 interface the card to the system data buss. Read and write enabling are controlled by signals generated as described above.

4.5.5 VRAM ADDRESSING LOGIC
(See drawing no. C045-04)

4.5.5.1 Addressing Counters

The address being accessed within the VRAM is determined by the state of counter chain B1-B5. These are up-down counters which provide the auto-increment (and auto-decrement) functions. The starting address for any operation is established by any access to the VRAM. This is achieved by the counters being parrallel-loaded by the ADSTB (Address Strobe) from Sheet 3.

Horizontal increment or decrement is achieved by pulses UP1 and DN1 clocking the low-order 9 bits of the counter chain. The 3 lowest bits are used to select the bit within the byte. Vertical increment or decrement is achieved by clocking the highest 8 bits of the counter.

4.5.5.2 Bit Selection

The 16 kilobyte VRAM card is bit addressable, that is each row of chip selects can be individually enabled.

For Byte mode operations, the BYEN signal is TRUE, disabling gates A10 and B10, forcing the Chip Select outputs, CS0-CS7, to their TRUE (High) state. This causes the whole byte to be written irrespective of the current bit position within the byte.

For Bit mode operations, only the bit determined by one-of-eight decoder C2 will be enabled.

4.5.5.3 Vertical Scrolling

Counter chain C2, C3 and C4 generate the 14 bit address for the VRAM display operation. Each time a byte is fetched into the FIFO (sheet 2) and INCA (Increment Address) pulse clocks the counters on to the next byte. The starting line is preset into counters C2 and C3 at the beginning of each frame by SYNR. The starting line number is latched by C6 by writing to $FCDC.

This number determines which display line will appear at the top of the picture. Note that as the data buffers on this card are non-inverting, the complement of the desired line number must be written to the scroll latch.

4.5.5.4 VRAM Address Multiplexing

Quad data multiplexers A1-A4 multiplex the address buss of the VRAM between processor accesses (addresses from counter chain B1-B5) and video display addresses (counter chain C2-C4).

Switching is done by the BADD2X signal which is derived from phase two of the processor to which access has been enabled.

## 4.6 Q025 16K BYTE MEMORY MODULE FUNCTIONAL DESCRIPTION

### 4.6.1 INTRODUCTION

The Q025 16 K memory is used as the video graphics RAM (VRAM) for the Graphics Display system. It is driven by the Q045 Graphics Display Controller card. The motherboard buss is broken between these two card slots so that the VRAM can be accessed by the Q045 without performing DMA cycles.

### 4.6.2 ADDRESSING LOGIC & ROW-COLUMN MULTIPLEXER
(Refer to drawing Q025-01)

#### 4.6.2.1 Address Decoding

MA14 and M15 are the two most significant address bits which are used to select one of four 16K blocks of memory via one half of one-of-four selector B1. A four section Dual-in-line switch package is provided to allow user block selection. The following base addresses are selected by closing one of the four switches:

| Switch # | Base Address |
|---|---|
| 1 | 0000 |
| 2 | 4000 |
| 3 | 8000 |
| 4 | C000 |

When used as a VRAM for graphics applications, a base address of 0000 is used, so switch 1 should be closed.

The other half of B1 decodes MA12 and MA13 to select one of four rows of memory.

#### 4.6.2.2 RAS/CAS Generation

Hex latch B3 is clocked by CA to capture the required Row Select, Read/Write and Refresh signals. When REF goes low (Memory Refresh cycle in progress) the CS pin (edge connector pin 75, chip select) of the module is forced high, disabling all RAMS. All RAS signals are forced into their active state (low) by B6 for memory refreshing.

Column address strobes are generated on every cycle. These are driven to the RAM array via inverters A7 and series termination resistors.

#### 4.6.2.3 Row/Column Multiplexers

Row-address/Column-address multiplexing is achieved by tri-state buffers A1,A2, which are enabled alternately by RA and CA.

### 4.6.3 RAM & DATA BUFFERS
(Refer to drawing Q025-02)

#### 4.6.3.1 RAM Array

The RAM chips are dynaric M.O.S. devices of 4096 x 1 organisation. Chip selects are brought out to the edge connector in eight groups so that they can be disabled during refresh cycles or enabled one at a time for bit-mode operations. These are connected to the CS output from A6 for normal Byte mode R.A.M. operation.

4.6.3.2 Data Buffers

The RAM chips have seperate data input and data outputs which are switched onto the bus of transceivers A3-A4 depending on the state of READ.

Data input is always enabled; writing is achieved by taking WRITE low.

## 4.7 Q148 LIGHT PEN INTERFACE - FUNCTIONAL DESCRIPTION

### 4.7.1 INTRODUCTION

The Q148 Light Pen Interface is used to generate light pen co-ordinate data from Hit and Touch signals coming from the Light Pen.

It achieves this by counting the horizontal bits and vertical lines as they are displayed and latching the instantaneous values when a Hit pulse arrives from the lightpen. The co-ordinates are then available to be read from the card by the processor.

The light pen is activated by touching the insulated end of the pen, which generates a Touch signal. The Interface can be configured to generate an interrupt when the Touch signal is activated.

The card can also be configured so that the Hit signal causes the picture information to be inverted, which generates a "cursor" on the display at the position the pen is currently "seeing".

The Hit signal from the pen is de-glitched by the interface so that random noise due to external interference will not cause false triggering.

### 4.7.2 Co-ordinate counters, deglitcher, P.I.A
(Refer to drawing Q148-Ø1)

#### 4.7.2.1 Co-ordinate counters and Latches

The current bit within the line (Ø-512) is counted by 9 bit counter chain A8, B8, C8. The bit rate clock BITCLK comes from the system buss and originates at the Q045 Graphics Controller Card. The 9 bits of data from these counters are latched by A7, B7 and C7 when a STB pulse occurs (deglitched Hit). The least significant bit of the count is gated onto the buss by POIL, and the remaining eight bits are gated onto the data buss by POIH.

The line counter D3 counts LINC pulses, which normally come from the bit counter chain via multiplexing circuitry on sheet 3. The eight bit line count is latched by B8 and C8 when a STB occurs, and can be read onto the data bus by LINE.

#### 4.7.2.2 Hit Deglitcher

Deglitching operates by ensuring that light pen hits are repeated a minimum number of times on sucessive display lines.

Counter D4 is normally in its terminal count state, counting being inhibited by TC being high, which forces CEP low. A Lightpen Hit pulse AHIT arriving at gate E5 will RESET the counter via its Master Reset, MR. The counter then procedes to count line pulses LINC. Once the desired number of lines, normally three, set up by HOFØ-HOF3 has been reached, the next AHIT pulse will cause a logic 1 to be clocked into flip-flop E6. On the next BITCLK this is propagated to the second flip-flop in E6, generating a STB pulse to clock the co-ordinate latches. If no Hit occurs during the third line after the first hit,

the count continues to its terminal state (16) without a STB being generated.

The STB generating flip-flop can be locked out for the rest of the line or the rest of the frame by the Reset pulse selected by multiplexer D7, which is controlled by the two low bits of Mode Select (MSØ and MS1).

4.7.2.3 Control P.I.A.

Peripheral Interface Adaptor B6 provides read/write ports for a variety of different functions. The A side is configured as outputs and are used for Mode Selection MSØ-MS6. The low nibble of the B side is used to control the number of lines ignored after vertical synch when operating in external synch mode. The high nibble of the B side determines the number of sucessive Hit lines required by the deglitcher to recognise a valid hit.

The P.I.A. is also used to generate interrupts. Two seperate interrupt outputs are possible, one for Touch and one for Hit. These are generated by the P.I.A. CA1 and CB1 inputs respectively.

4.7.3 Address Decoding, Timer and Data Buss Control

4.7.3.1 Address Decoding

The Light Pen Interface occupies 16 bytes of memory space from $E200 to $E2DF. Addresses in this range are decoded by NAND gate A1. As well as VMA (Valid Memory Address), one of the Processor Address signals may be gated in at this point by link option W1. This allows the card to operate either with both processors or processor unique. The E2DX signal is latched by hex D-type flip-flop A3, along with R/W (Read Write) and the low four address bits.

Further address decoding provided by C1, C2 and B2 generate the enable signals required to read co-ordinates, POIL, POIH and LINE and to enable the chip-selects of the P.I.A. and Timer.

4.7.3.2 Timer

An M6840 Timer is provided for general system use. This device contains three independent 16 bit counters which can be configured under software control to count external events or internal clock pulses. Counter 1 is clocked by LINC to count Lines, counter 2 is clocked by FR to count frames, and timer 3 is clocked by a 1 MHz system timing signal to count microseconds.

For full operational specifications of the 6840 refer to the manufacturers data sheets.

4.7.3.3 Data Buss Interface

The card is interfaced to the system data buss by two quad buss tranceivers. These are configured so that data normally passes from the system to the card (as used for WRITE operations). During a cycle the direction is reversed by the READ signal so that data can be read from the card.

4.7.4 MODE SELECTION AND EXTERNAL SYNCH.
(Refer to drawing Q148-03)

4.7.4.1 Mode Selection

Seven bits of mode control are used by the card and must be configured by the driving software. The bits and their functions are:

MS0,MS1 Select Hit Lockout-
0= Lockout for rest of frame
1= Lockout for rest of line
2= No lockout

MS2,MS3 Select Synchronisation Source-
0= Graphics Controller Card
1= T.V.T. Card
2= External Composite Synch

MS4 0= Touch for Hit

MS5 Graphics Invert

MS6 Cursor On

Mode slect bits 0 and 1 are dealt with on sheet 1 (above).

MS2 and MS3 are used to control two dual one-of-four data selectors, D8 and E8. Within Line Reset (WLR) pulses are multiplexed between the Graphics Reset input from the buss (GR), TVT Synch input from the buss (TVTSYN), and Local Synch from the Synch Seperator (LOCSYN). The Bit Clock (BITCLK) is multiplexed between Graphics Bit Clock from the buss (GBIT), TVT Bit Clock from the buss (TVTBIT) and a 4MHz clock generated by gating the BCA and BCAS system timing signals. Line Increment (LINC) is multiplexed between Line Finish from the bit counter (LFIN), TVT Line Synch from the line synch seperator driven by the TVT Synch (TVTSYN) and Local Line Synch pulses from line synchs seperated from the external composite video input (LOCSYN).

4.7.4.2 External Synch

An external composite video source can be used to synchronise the lightpen interface.

The video is fed to amplifier Q2, Q3 which raises the amplitude to about 3 volts p-p. The video is then stripped by Q1 to provide a synch-only signal to Schmitt trigger E7. This synch is then inverted by E4 to provide the Local Synch signal LOCSYN. Vertical synch pulses are seperated from the composite synch by one-shot E3 and flip-flop E2. The one-shot is configured to generate an output puls about 10 milliseconds wide for each negative-going input pulse. If the pulse finishes after the one-shot times out a logic one is clocked through the flip-flop, signalling a vertical synch.

The vertical synch presets the second half of flip-flop E2causing the Q output to go high and a pulse to be generated by D2. This becomes the Frame Reset pulse FR. The line counter (sheet 1) is reset to zero, and incremented each line. When the start line count established by mode control bits ST0 to ST3 matches bits 2 to 5 of the line count,

exclusive-or gates D6 generate a Reset to flip-flop E2, which in turn generates a second frame reset pulse, reseting the line counters.

4.7.4.3 Hit, Touch Receivers

The Hit and Touch lines from the lightpen are T.T.L. compatible signals, asserted low. They are terminated at the receiving end by resistor networks R19-R22. Depending on the state of mode select bit 4 (Touch for Hit) the Touch signal may be ANDed with the Hit signal to generate a valid Hit pulse (AHIT).

Mode select bit 6 (Cursor) determines whether the Invert output will be strobed by Hit pulses to form a cursor.

Mode select bit 5 causes the picture to be inverted (negative) when set to a 1.

Note that gating is arranged to disable the cursor when the Touch is asserted. This is to ensure that the pen has something to "see" when activated.

## 4.8 CMI02 MASTER CARD - FUNCTIONAL DESCRIPTION

### 4.8.1 INTRODUCTION

The CMI02 Master Card performs a variety of functions including control of the eight channel cards, analogue to digital conversion for sound sampling, and timer functions for sequencer and Music Composition Language. It occupies the first slot from the left in the card cage of the C.M.I. Mainframe.

This card occupies 64 bytes of processor address space. It can be accessed by either processor. The address map is as follows:

| ADDRESS (Hex) | FUNCTION |
|---|---|
| E000-E01F | CHANNEL CARD REGISTERS |
| E020 | CHANNEL MASK DATA REGISTER (P.I.A) |
| E021 | CHANNEL MASK CONTROL REGISTER (P.I.A.) |
| E022 | MASTER TUNING DATA REGISTER (P.I.A.) |
| E023 | MASTER TUNING CONTROL REGISTER (P.I.A.) |
| E024 | A.D.C. DATA HIGH BYTE |
| E025 | A.D.C. DATA LOW BYTE |
| E026 | HALT PROCESSOR 1 |
| E027 | UN-HALT PROCESSOR 1 |
| E028 | LEVEL CONTROL DATA REGISTER (P.I.A.) |
| E029 | LEVEL CONTROL CONTROL REGISTER (P.I.A.) |
| E02A | FILTER CONTROL DATA REGISTER (P.I.A.) |
| E02B | FILTER CONTROL CONTROL REGISTER (P.I.A.) |
| E030 | P.I.C.U. ENABLE CURRENT STATUS |
| E031 | INTERRUPT PROCESSOR 1 |
| E032 | CLEAR PROCESSOR 1 INTERRUPT |
| E033 | INTERRUPT PROCESSOR 2 |
| E034 | CLEAR PROCESSOR 2 INTERRUPT |
| E038-E03F | TIMER REGISTERS (6840) |

4.8.1 Address Decoding, Channel Selection, VRAM Switching, Master Tuning Register.
(Refer to Drawing CMI02-01)

#### 4.8.1.1 Address Decoding

Addresses in the range E000-E03F are decoded by NAND gate A1. Once addressed, the SEL (Select) signal is latched by D-type flip-flop C1. Channel card addresses in the range E000-E01F are decoded by NOR gate C2 to produce CHSEL (Channel Select).

#### 4.8.1.2 Channel Selection

All eight channels occupy the same address space and channel selection is achieved by establishing a mask of desired channels in the B side of P.I.A. BC9 (Channel Mask). NAND gates A10 and B10 enable one or more channels when a WRITE to a channel card address is performed. It is not possible to read from more than one channel at a time without buss contention, so circuitry is provided to protect against crashes which may result from a software bug which causes inadvertant reading from multiple channels. ROM A9 is programmed to generate a logic zero

if more than one bit is set in the channel mask. If a READ is attempted under these conditions, the CHSEL is inhibited.

4.8.1.3 VRAM Switching

The Video RAM of the Graphics Display System occupies 16 Kilobytes of address space from 8000-BFFF (hex). In order to make this address space available for use as system RAM when the VRAM is not being accessed, switching is provided by the Master Card.

Addresses in the range 8XXX during Processor 1 cycles are decoded by 4-input AND gate B1. These cause VREN to be asserted, which disables the VRAM and enables the RAM via NOR gate D9 and inverter A8. This means that Processor 1 never accesses the VRAM.

If control bit CB2 of P.I.A. BC9 is SET, the VRAM is permanently disabled and the RAM enabled. To access the VRAM, CB2 must first be CLEARED.

4.8.1.4 Master Tuning Register

The B side of P.I.A. BC9 is configured as outputs, the data written to it being used as Master Tuning control (MT0-MT7) by the Master Pitch generator (Sheet 2).

4.8.2 Interrupt Control, Master Oscillator, Memory Control
(Refer to Drawing CMI02-02)

4.8.2.1 Interrupt Control

The eight channel cards generate Processor 1 interrupts which occupy the eight interrupt levels supported by the C.P.U. Control Card Q032. To support the remaining interrupts, a second P.I.C.U. (Programmable Interrupt Control Unit) is provided on the Master Card. It is acscaded with the one on the Q032 card.

The P.I.C.U. C8 normally provides the three highest priority interrupts to Processor 1. These are, IRQSYN from the keyboard A.C.I.A., TIMINT from the 6840 timer, and interprocessor interrupts. The current interrupt priority level is written to the P.I.C.U. by a WRITE to E030 (hex). If an interrupt of a higher priority arrives, the INT output of the P.I.C.U. will be asserted (low), setting the flip-flop formed by gates A10, B2 and generating a Processor 1 Interrupt Request (IRQ1). The level of the interrupt is presented to the Interrupt Address Buss IA01-IA21. This address is used as bits 1 to 4 of the memory address when fetching the interrupt vector.

The interrupt latch is cleared when a new interrupt status is written to the P.I.C.U.

4.8.2.2 Master Oscillator

Transistor Q1 and crystal Y1 form a 34.29 MHz oscillator from which the channel card pitch reference is derived. Flip-flop E10 divides the output of the oscillator by 2 to provide a symetrical square wave at 17 MHz. This is fed to rate multipliers C10 and D10, which give a small range of frequency control, as determined by the data from the

Master Pitch register (sheet 1). The output of these rate multipliers is fed to all channel cards via buffer A7.

4.8.2.3 Memory Control

Counters E8 and D8 are clocked by the 17 MHz signal from the crystal oscillator and their output addresses timing ROM B8. This ROM generates the timing signals required by the Waveform PAM on the Channel Cards. They are SREF (Refresh), SRA (Row Address), SRAS (Row Address Strobe), SCAS (Column Address Strobe). The outputs of the ROM are latched by quad flip-flop B7 and buffered onto the buss by A7.

4.8.3 Analogue to Digital Converter
(Refer to Drawing CMI02-03)

The Analogue to Digital converter is an AD571 (D7), of 10 bits accuracy. The sample rate is determined by the frequency set up by the Channel Card in the Channel 1 position of the Mainframe. This clock arrives at the Master Card edge connector pin 44. ADM (A-D Mode) is normally low, enabling the ADCLK (A-D Clock) through to one-shot D2. This one-shot generates the 2 uS pulse required by the AD571 to start a conversion cycle.

When waiting for a conversion cycle, Processor 1 halts itself by accessing E026 (hex). This generates a JAM strobe, CLEARing flip-flop D3 which causes HLT (Halt) to go low.

When the conversion is complete (approximately 30 microseconds later) the DR (Data Ready) output of the AD571 goes low, forcing the output of NOR gate D9 High, clocking the data latches C5 and C7, which capture the data ready for reading by the processor. At the same time as the conversion is completed, flip-flop D3 is clocked, setting it. The Q output is forced LOW again, removing the HALT condition from Processor 1 and allowing it to run again and read the A-D data. If Processor 1 is held halted for more than 100 mS, one-shot D2 times out, allowing it to run again. This is to protect against system hang-up in the event of an A-D failure.

The audio signal arrives at the Master Card at pin 9 of the 10-way ribbon cable plugged into the front of the card. Sample-and-hold E9 is gated by the DR (Data Ready) signal from the DAC to ensure that the signal input to the DAC remains constant while a conversion is in progress.

4.8.4 A-D Filter System
(Refer to Drawing CMI02-04)

Low-pass and high-pass filters are provided for limiting the bandwidth of the signal being fed to the Analogue to Digital converter. The cutoff points of each are individually controllable.

Signal arriving at the Master Card at pin 1 of the 10-way ribbon connector is attenuated by MDAC E4. The attenuation is controlled by the data written to the A side of P.I.A. DE5. Op-amp F3 in combination with CMOS switches E1, F1, F5 form the low-pass filter. The cutoff frequency is determined by the resistors selected by the switches, which are addressed by the low four bits of the B side of P.I.A. DE5.

The output of the low-pass filter is available for monitoring at test point TP9.

Op-amp E7 together with switches F7, F8 and F10 form the high-pass filter. The cutoff point of this filter is controlled by the high four bits of the B side of P.I.A. DE5.

The plus and minus supplies for the CMOS switches are provided by zener diodes ZD1 and ZD2. 5.6 volt zeners are used so that the supplies to the switches will excede 5 volts to prevent distortion of the signal which can be up to 10 volts peak-to-peak.

## 4.9 CMI01 CHANNEL CARD - FUNCTIONAL DESCRIPTION

### 4.9.1 INTRODUCTION

The Channel Cards are the audio generation and manipulation system of the C.M.I.

Up to eight cahnnel cards may be installed. All eight cards are identical and interchangeable. Their assignment (1 to 8) is a function of which slot they are plugged into in the C.M.I. Card Cage.

Each Channel Card contains 16 kilobytes of waveform RAM in which sounds are stored. Circuitry is provided to clock out this memory to a digital to analogue converter, also located on the channel card.

The speed at which the memory is clocked out, and hence the pitch of note produced, is controlled by a 12 bit number written to the pitch register on the card.

A tracking filter follows the DAC. This automatically follows the frequncy of the channel, filtering out unwanted noise at a certain number of octaves above the fundamental frequency. The ratio of the filter cutoff to the pitch beinbg played is controllable by writing to the filter control latch (used by the FILTER control on Page 7 of the C.M.I. system software.)

The channel card occupy 32 bytes of memory space from E000 to E01F. The 16 kilobytes of waveform RAM are accessed by a single "porthole" at E000. Auto-incrementing hardware causes data to be read or written to each byte sequentially as repeated accesses are made to this location. The starting byte number is estabilished by writing to a special register.

As all eight channels live at the same address, a mechanism for selecting which channel(s) are accessed is provided. This is controlled by the Channel Mask Register, located on the Master Card CMI02.

Audio output is taken from the 10-way ribbon connector on the front of each channel card. This is in the form of a balanced signal. The signal is also available at the test points at the front of each card. Refer to the Diagnostic Software section of this manual for full details.

Power for the analogue cicuitry (+ and - 15 volts) is fed to the Channel Cards via the same ribbon cable.

Details of Channel Card operation are proprietary information which is not available outside the Fairlight factory in Sydney.

## 4.10 CMI04 AUDIO MODULE - FUNCTIONAL DESCRIPTION

### 4.10.1 INTRODUCTION

The Audio Module interfaces the audio input/output connectors on the rear panel of the C.M.I. mainframe with the appropriate internal circuitry.

Functions include buffering of audio outputs from the channel cards, generation of a mixed line output, provision of a monitor amplifier for driving a monitor speaker or headphones, processing of synch input and output signals, and supply of power to the channel cards.

### 4.10.2 MIXER, LINE DRIVERS
(Refer to Drawing CMI04-01)

#### 4.10.2.1 Mixer

Audio from the channel cards arrives at the Audio Module by means of a fifty-way ribbon cable. This cable is split down to eight seperate groups which plug into the channel cards.

The signal is balanced, to minimise noise pickup. Each channel is received by a differential amplifier which removes common-mode noise. The channels are then mixed down by eight resistors feeding a virtual-earth summing amplifier IC5 to form the Monitor output.

#### 4.10.2.2 Line Drivers

All eight channels, plus the monitor output, are buffered before being fed to the appropriate output via a 330 ohm isolation resistor. An op-amp inverter provides an anti-phase signal for each balanced output.

### 4.10.3 MONITOR AMP, INPUT AMPS, SYNCH IN/OUT
(Refer to drawing CMI04-02)

#### 4.10.3.1 Monitor Amplifier

Signal from the output of the mixer (sheet 1) is fed via the Monitor potentiometer (on the rear panel of the Mainframe) to the monitor amplifier. It arrives at pin 30 of the edge connector, from where it is amplified by audio amplifier IC12. Power boost for this amplifier is provided by transistors Q1 and Q2.

Pulses from the Click Monitor potentiometer are mixed into the Monitor amplifier by resistor R3 and capacitor C14.

#### 4.10.3.2 Input Amplifiers

The Microphone Input is amplified by op-amp IC7. The noise of this stage is reduced by using transistors Q3 and Q4 as the gain elements of the op-amp. Transistors Q5 and Q6 form a current source for the differential input stage.

Line input is buffered and un-balanced by differential amplifier IC8.

Output from the Mic pre-amp or Line input amplifier is routed to the Master Card depending on the setting of the MIC/LINE switch on the rear panel of the Mainframe.

After filtering on the Master Card, the audio signal is returned to the Audio Module via pin 8 of the ribbon cable connector SØ2. It is buffered by op-amp IC9 and fed to the FILTER OUT connector on the rear panel, as well as the INT/EXT ADC selector switch.

4.10.3.3 Synch In/Out

The Click signal from the Master Card is a symetrical square wave. It arrives at pin 7 of SO2. It is filtered by IC1Ø and associated components, resulting in a pulse waveform which is fed to the Click Output on the rear panel, and also the Click potentiometer on the rear panel.

Synch input to the Mainframe arrives at pin 72 of the edge connector SO3. IC15 is configured as a Schmitt Trigger which squares up the incoming waveform and rejects noise by virtue of its hysteresis. Zener diodes ZD2 and ZD3 clip the output of the op-amp to limit the excursion to about + and - 4.5 volts. Resistor R1Ø4 and zener diode ZD1 further limit the excursions of this signal to approximately +4 and -.7 volts, suitable for feeding to the Master Card via ribbon cable connector SØ2 pin 6.

4.1Ø.4 POWER SUPPLY

Raw D.C. supplies of approximately + and - 2Ø volts arrive at the card via connector PL4. When power is first applies, relay RLA is open and no power is fed to the regulator ICs. As capacitor C5Ø charges, the current through transistor Q8 increases until the voltage accross resistor R1Ø8 excedes .7 volts. Transistor Q7 then switches on, pulling the base of Q8 up to the supply, which causes relay RIA to close.

Power is then applied via RLA1 and RLA2 to the regulator ICs IC13 and IC14.

The purpose of this delay is to mute the audio outputs until the processor system has started up and initialised the channel card hardware.

## 4.11 CPSA D.C. POWER SUPPLY ASSEMBLY - FUNCTIONAL DESCRIPTION

### 4.11.1 INTRODUCTION

The D.C. Power supply provides regulated power for all the circuit boards within the C.M.I. card cage, the floppy-disk drives, the music keyboard and alphanumeric keyboard.

Power for the analogue (audio) circuitry is provided by regulators located on the Audio Card CMI04, mounted inside the rear panel of the mainframe. This provides plus and minus 15 volts for the Channel cards, Master Card and Audio card. The remainder of the digital electronics is supplied by regulators mounted on the rear of the card cage. This provides -5, +12 and -12 for the cards within the card cage, and +24 and +5 for the floppy disk drives.

### 4.11.2 UNREGULATED SUPPLIES
(Refer to drawing MC001-01)

The Unregulated Supply assembly is constructed as an integral part of the C.M.I. Card Cage assembly. It comprises a transformer, rectifiers and filter capacitors. A schematic diagram of the assembly is shown on drawing MC001-01.

Transformer T1 is supplied with A.C. mains via a fuse, mains switch, line filter and voltage selector. A 10 V.A.C. winding supplies bridge rectifier DB1 to give 10 volts raw D.C. across C1 at its full load of 20 Amps maximum. Its fuse is located on the regulator assembly P.C.Board.

A 28 V.A.C. winding feeding bridge rectifier DB2 provides +40 volts, smoothed by C2 and fused by F2. A centre-tapped 32 V.A.C. winding in conjunction with DB3 supplies plus and minus 20 volts to smoothing capacitors C3 and C4 and fuses F3 and F4 respectively.

A 33 V.A.C. winding feeding bridge rectifier DB4 and capacitors C5 and C6 provide the plus and minus 20 volts D.C. to the regulator on the Audio Card CMI04.

### 4.11.3 REGULATOR 5 VOLT 18 AMP
(Refer to drawing CPSA-01)

This regulator is part of the regulator assembly located at the rear of the C.M.I. Card Cage.

IC1 is the regulating element of the circuit. Transistor Q2 senses the current drawn by IC1, driving parellel transistors Q3 to Q6. Equal current sharing is ensured by emitter resistors R7-R10.

Current limiting is provided by germanium transistor Q1, which uses the drop across sensing resistor R1 as a current sense. Short circuit current is limited to approximately 20 Amps, regulation falling off above about 18 Amps.

Over-voltage crowbar protection is provided by SCR1. If the output of the 5 volt regulator rises above 6 volts zener diode ZD1 conducts, switching on the S.C.R. This protects components using the 5 Volts

supply in the event of regulator malfunction or an inter-supply short-circuit. If the crowbar circuit does switch on, 15 Amp fuse FS1 will blow.

4.11.4 + 12 VOLT, 24 VOLT SUPPLIES
(Refer to drawind QPSA-Ø2)

The plus and minus 12 volt supplies are simply regulated by integrated circuits IC3 and IC4 respectively. The +12 volt supply is current-limited to about two amps by the regulator I.C. IC3. The -12 volt supply is current limited to about 1 amp by regulator I.C. IC4.

The 24 volt supply is regulated by integrated circuit IC2. Transistor Q7 boosts the available current to about 3 Amps. Zener Diode ZD1 provides a voltage drop to protect the regulator I.C. from excessive input voltage.

## 4.12 C036 FRONT PANEL CONTROL

*** DATA NOT YET AVAILABLE ***

# 5.0 TROUBLESHOOTING

## 5.1 Introduction

The C.M.I. system relies on a complex interaction of hardware and software for proper operation. It is often difficult to differentiate between hardware faults, software bugs and operator errors. Before attempting repair of the Mainframe, establish that the fault is definitely a hardware fault in that unit. If in doubt, try the same series of operations on another system of the same revision level to ensure it is not a software bug and check with the Users Manual to ensure it is not operator error.

Refer to the C.M.I. System Service Manual for information on how to ascertain that the fault lies within the Mainframe itself and not one of the other system units.

Due to the complexity of the system, this manual does not attempt to present an exhaustive list of faults and repair procedures. Instead, the detailed descriptions (above) should provide service personnel with a thorough understanding of the hardware so that the problem area can be identified.

Extensive diagnostic software is provided to thoroughly test most of the hardware. Of course, in order to run the diagnostics the computer section must be running at least to the stage of loading and executing the software. Use of the diagnostic software is described in detail in section 6 (below).

A guide to troubleshooting the major components of the Mainframe follows:

## 5.2 Power Supply

A fault in the power supply will usually result in complete failure of the system (the computer does not run, so no message is displayed on the screen). An exception to this is a failure of the analogue supply (+/- 15 volts to the channel cards, master card and audio card). In this case, the C.M.I. should appear to function normally although no sound will be produced.

Three L.E.D.s are provided on the front panel of the C.M.I. to indicate the state of each of the digital supplies, +12, -12 and 5 volts. These are the supplies to the cards in the card cage, supplied by the Motherboard. The L.E.D.s will not light if the relevant supply drops below two-thirds of the nominal voltage. Note that these L.E.D.s pick up their supplies via the ribbon cable connected to the Q032 card, so it is possible that a fault in the Q032 could cause the L.E.D.s to malfunction.

Fuses for the +24 volt supply (disk drives) and +/- 12 volt digital supplies are located on the transformer cover plate at the left-hand end of the card cage. They are accessed by hinging down the front panel. The +/- 12 volt fuses actually protect the raw D.C. supply to the 12 volt regulators (see 4.11, QPSA below). As this raw supply also powers the music and alphanumeric keyboards, a fault in either of

these units could blow the fuse. The +/- 12 volt supplies are current limited so that a fault on a circuit card will not normally blow a fuse.

The raw supply to the +5 volt regulator is protected by a 15 amp cartrige fuse mounted on the regulator P.C. card. This fuse should never blow except in case of catastrophic power supply failure. See 4.11 CPSA (below).

All other fuses are located on the rear panel of the mainframe.

In the event of a power supply failure, be suspicious that the failure may have been caused by a malfunction elsewhere, or incorrect setting of the mains voltage selector (on the Mainframe rear panel).

5.3 Computer Section

A failure in the computer section may result in permanent or intermittent malfunction of the system.

If the system will run to some degree (i.e. load a disk and respond to commands) the diagnostic software described below should be run to localise the fault and the offending card can then be replaced.

If the system will not run at all (will not load the diagnostic disk) start by checking the following:

1) Halt/Run switches on the front panel must be in the Down (RUN) position.
2) Terminal Speed setting on the front panel must be set to 9k6.
3) Mains voltage selector on the rear panel must be set correctly.
4) Power must be applied, as indicated by the three L.E.D.s on the front panel.
5) The Sysytem Disk must be in good order (as indicated by testing in another system) and inserted correctly.

If these items are all in order, but the system disk will not load, confirm that the fault lies in the Mainframe by disconnecting everything except the A.C. supply from it and trying to load the disk again.

If the disk will still not load, the system should be "stripped down" until operation is restored. Remove cards in the following order attempting to load the disk after each stage:

1) Remove all eight channel cards (CMI-Ø1)
2) Remove the lightpen card (Ç148)
3) Remove the master card (CMI-Ø2)

If the disk will still not load, substitute the remaining cards with known good spares one at a time. If the fault persists, the problem must be in the power supply, disk system, motherboard or cabling. Refer to Section 7 (Motherboard Signals) and Section 8 (External Connections) below, for details of motherboard and external signals.

## 5.4 Disk System

The Disk system consists of three sections - the floppy-di controller card CFC2, interconnecting cables, and the two floppy-di drives themselves.

A fault in the controller card or cabling will generally result hard disk errors or total failure to access disks. Soft intermittent disk errors will usually be caused by a faulty misaligned drive.

A toggle switch mounted on the front edge of the controller ca reverses the drive select signals to the drives so that the logic drive numbers can be swapped for diagnostic purposes. For example, a disk error is reported during boot-load, the drives can be swapp (switch down) and the system disk inserted in the right-hand drive. it then loads sucessfully, the left-hand drive is faulty. If the fau persists, the fault is in the controller, cabling or power supply unless the system diskette itself is faulty.

Refer to the Fairlight Disk System Service Manual for full details disk drive maintenance.

## 5.5 Channel Cards

Incorrect operation of individual channels is caused by a fault channel card or audio card.

Comprehensive diagnostic software is available for testing the channe cards. The digital circuitry is tested automatically, and the analogu circuitry requires waveform measurement using an oscilloscope.

Channel selection is performed by the Master Card (CMI-C2). A fault i this area will show up as a digital failure of one or more channe cards when the diagnostic software is run.

In case of an audio fault in one particular channel, it is not alway clear whether the fault lies in the channel card or the audio card This can be resolved by swapping the suspect channel card with a goo spare, or with another good channel card in the same Mainframe. If th fault remains in the same channel output, the fault is in the audi card, or possibly the ribbon cable connecting the channel card to th audio card.

## 5.6 Master Card

Special Master Card diagnostic software is provided to test al functions (see section 6 below). The Master card is responsible fo the following major functions:

### 5.6.1 Channel Card Selection

Faulty channel card selection will show up as channel card failures when running the digital tests of the Channel Card diagnostics. If a channel card fault is detected by the diagnostics, and the fault persistes when the card is changed, then the master card may be at fault and should be exchanged for a good spare.

### 5.6.2 Channel Card Master Clock

The crystal oscillator located on the master card provides the master pitch reference and memory timing signals for all channel cards. These signals for all eight channel cards are bussed together. A fault in this area will cause identical faults in all channels, manifested primarily as Memory or Pitch test failures.

### 5.6.3 Analogue to Digital Conversion

Improper operation of the Sound Sampling (Page 8 of the C.M.I. System Software) will be caused by a fault in the Master Card, Audio Card, or interconnecting cabling.

As a first step, the Master Card should be exchanged with a good spare. If the fault persists, the Audio Card should be replaced next. Finally, the interconnecting cables should be checked using the Mainframe Wiring Diagram (Drawing number MC00l-01), Audio Card Functional Description and Master Card Functional Description as a guide.

### 5.6.4 External Synchronisation and Timer

Improper operation of the Synch Input or Click Output function (M.C.L. or Page 9) can result from a fault in the Audio card or Master Card, or the 10-way ribbon cable connecting the two together.

Diagnostic software is provided for testing the operation of both the input and output. Refer to section 6 (below) for full details.

The fault should be isolated by replacing the Master Card with a good spare, followed by the Audio Card, and finally the interconnecting cable.

## 5.7 Audio Card

The Audio Card (located inside the rear panel of the mainframe) provides buffering for the analogue signals entering and leaving the Mainframe, as well as regulating the +/- 15 volts power supply to the analogue circuitry.

The following types of fault will usually indicate a faulty Audio Card:

1) Audio faults appearing in a particular channel which are not cured by exchanging channel cards.

2) The Mixed Line Output does not function properly, although each individual channel output is correct.

3) The Monitor speaker output or Headphone output is faulty.

4) Sound sampling using Mic input does not work, but the Line input does (or vice versa).

The following faults may be caused by an Audio Card malfunction or some other fault:

1) Synch input or output does not function properly.

2) Analogue power supply (+/- 15 volts) incorrect.

3) Improper opereration of an individual audio channel.

# 6.0 DIAGNOSTIC SOFTWARE

## 6.1 INTRODUCTION TO DIAGNOSTIC SOFTWARE

This section describes the set of diagnostic test programs available on disc for testing and debugging all the plug-in circuit modules of the Fairlight Computer Musical Instrument.

### 6.1.1 Running the Diagnostic Disc

The diagnostics run under the QDOS operating system. They are therefore supplied on a QDOS system disc which should be loaded into the CMI instead of the usual CMI system disc immediately after power-up or RESTART.

As soon as the disc drive door is closed, the CMI will load QDOS automatically and display a sign-on message giving version and revision numbers.

The QDOS prompt will then be displayed. This is just an equals sign "=" on a line of its own. This indicates that the computer is ready to accept a command.

For further details of the QDOS operating system features, refer to the QDOS User's Guide.

### 6.1.2 Running the Test Programs

Most of the diagnostic programs make use of a common command interpreter for operator control, so there is a uniform command syntax employed throughout, and several test options available as standard. Tests may be run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

where the <test name> is as described in each section. Options are of the form

<O>=n  where <O> is a single character and n is an integer.

Standard options are

P=n  Repeat test command n times. Using "C" instead of an integer initiates continuous testing.

N=n  Select test number n. There are usually several test commands with the same name. By default all tests are executed sequentially but single tests or subsets of the available tests can be specified.

e.g. N=1  Test no. 1 only
N=1,3,5  Tests 1, 3 and 5
N=4-7  Tests 4 to 7 inclusive

Some tests, which require a waveform to be observed before terminating wait for the spacebar to be pressed or proceeding to the next test.

To obtain a reminder of what tests are available from the curren test program being run, type

LIST<CR>

To repeat the last test, just type

R<CR>

If an error condition occurs, a moderately helpful message is printe on the console and the program returns to the command interpreter Successful tests terminate without comment and return to th interpreter or proceed to the next test as soon as completed. Certai tests require the user to check waveforms with an oscilloscope an will not terminate or proceed to the next test until the spacebar i pressed.

### 6.1.3 Measurement Tolerances

A tolerance of +/- 15% is acceptable for most voltage or frequenc measurements. Filter attenuation levels are harder to control and ma be subject to +/- 20% variation. Changes to analog circuitry i design revisions may also effect level measurements. Values quote here are valid for the revisions referred to in the text.

## 6.2 Channel Card Tests

A program for testing CMI channel cards is CMITST.CM which can be run by typing

CMITST

with the CMI diagnostics disc in drive Ø.

It can test channel cards individually or up to eight at a time. There are eight different tests within CMITST, which each exercise a different part of the channel card.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

A "C=n" option is avilable for all tests, which specifies the channel number(s)to be tested, in the range 1 to 8. Default is 1. Multiple channel numbers can be specified separated by commas or a hyphen.

e.g. FILT;C=3
FILT;C=1-4
FILT;C=3,5

One side of the balanced analog output of the channel card is available at test point 6 (TP6) at the front of the card. The row of test pins is numbered from 1 at the bottom. Pins 1 and 2 are connected to digital ground, 3 and 4 to analog ground.The other side is available at test point 5. Measurements quoted in this text refer to TP6. However if a complete CMI is being tested, it may be more convenient to use the Fairlight Analog Tester box (see section 6.10.3 for how to connect it to the CMI and an oscilloscope). Waveforms observed from the tester will be of the same form as TP6 but different levels. Refer to the Waveform Summary (section 6.11) for Analog Tester levels.

Note that Fairlight DO NOT release schematics of the Channel Card as all repairs are done on a return-to-factory basis.

Board component references are for the Revision 7 channel card and this section describes CMITST Revision 1.3

CAUTION: WHENEVER CHANGING OR REMOVING THE CMI MASTER CARD OR CHANNEL CARDS, OR PLUGGING RIBBON CABLE CONNECTORS ONTO THESE CARDS, ALWAYS SWITCH OFF POWER FIRST. FAILURE TO DO SO WILL ALMOST CERTAINLY CAUSE HARDWARE DAMAGE!

### 6.2.1 Filter Tests

Test name: FILT
No. tests: 15
Purpose: Tests the basic playback facility of the channel card and the software-controlled tracking filter.

# 6809 CMI DIAGNOSTIC TESTS

5th March 1984.

## BASIC SYSTEM CHECK PROCEDURE

The following tests perform tests on the basic CMI hardware. The hardware components tested are:

- Diagnostic diskette
- Main memory
- Master card
- Channel cards
- Interrupt hardware
- Disk drives
- Video

See later sections for additional tests.

Procedure:

| | |
|---|---|
| CHAIN DISKETTE | (this test checks the diagnostic diskette) |
| CHAIN CMITEST | (tests Memory, Master, Channels, Interrupts) |
| DSKTST | (tests disk drives - see Service manual) |
| CHAIN AUDIO | (tests each channel for an audible output) |
| CHAIN VIDEO | (tests graphics/lightpen card;<br>NOTE: After typing "CHAIN VIDEO" press C, this causes a completely green screen, the lightpen can now be pointed to the screen and tested.<br>Press "ESC" key, this starts the Video Ram test, which causes random patterns on the screen. |

NOTE: If any of the above tests generate an error, an appropriate error message will be displayed.

## SPECIFIC TESTS

These tests check specific CMI cards or optional hardware.

These tests cover the hardware listed in the above section plus

- AIC card
- Printer
- Channel card analog hardware

Procedure:

| | |
|---|---|
| CHAIN AIC | (tests the inputs and the outputs of the AIC,<br>NOTE: the inputs and respective outputs must be connected together. |
| PRINTER | (produces a diamond shape, made out of a regular pattern of characters. Press "ESC" key to stop the test) |
| CHAIN ANALOG | (tests the analog hardware of the CMI, see Service manual) |

For each test a fundamental sine wave is loaded into two segments of waveform memory, and a program-specified harmonic is loaded into the following two segments. The segments are then replayed continuously (by segment looping) with the tracking filter cutoff set to achieve approximately a 2:1 attenuation between the fundamental and harmonic. The output level of the fundamental at TP6 should be 3.4V p-p.

After each of the 15 tests the program will halt until the space bar is hit so that the channel card output can be observed.

Test name: FILTD
No. tests: 3
Purpose: Tracking filter test with operator settable parameters.
Options: F=n Filter setting. Range 1-15, default 8
H=n Harmonic number. Range 1-32, default 16

This is basically the same as FILT, but with additional operator control. The fundamental used for tests 1-3 are 200Hz, 1000Hz, and 5000Hz respectively. The same frequncy shifting is used as in the FILT test, but the harmonic may be specified by the user as a multiple of the fundamental, as can the filter setting.

6.2.2 Waveform Memory Tests

Test Name: MEM
No. tests: 8

Test No.1 - "Read-write 0"
Purpose: Tests memory read-write atility.

First the waveform address counters are reset (G1-G3) then the entire memory is written with zeros. The address count is automatically incremented after each write by having LOAD asserted and PUN not asserted. Memory is read back in the same way to verify data.

Test No.2 - "Read-write FF"
Purpose: Tests memory read-write atility.

Writes $FF sequentially to entire memory and reads back to verify as in test 1.

Test No.3 - "Read-write and Refresh AA"
Purpose: Tests memory read-write atility.

Writes $AA to the entire memory, executes a delay loop for 5 seconds then verifies the contents of memory as in test 1.

Test No.4 - "Channel-Segment-Byte Uniqueness Forward"
Purpose: Checks that each byte in 16K memory of each channel card being tested can be addressed uniquely.

Memory is filled with 4-byte uniqueness patterns. Each pattern consists of the channel mask selecting that channel, the segment number being written to, and the double-byte offset of the first byte in the pattern.
Each channel memory is then read back in the same order to verify the patterns.

Test No.5 - "Channel-Segment-Byte Uniqueness Reverse"
Purpose: Addressing uniqueness.

This test is identical to No. 4 except that channel memories are filled beginning with channel 8 instead of channel 1. This in case a fault on channel 1 is causing a fault to appear on another channel.

Test No.6 - "Segment Random Access using Load"
Purpose: Tests ability to preset waveform segment counters.

Waveform segment counters (ICs G1,G3) are preset from the WS outputs of PIA FG5. This test can only be performed after test No.5 since it reads the uniqueness patterns to check that the correct segment has been selected.
A bit-swapping routine is used to generate a set of 127 non-sequential segment numbers. Each segment preset is loaded when the

ICAD signal (also from PIA) is toggled, and the second byte of the uniqueness pattern at that preset is read to check the segment number.

Test No.7 - "Segment Random Access using Run"
Purpose: Waveform segment presettability.

Tests waveform segment preset as in test 6 but preset is loaded when RUN signal toggles.

Test No.8 - "Sequential Access"
Purpose: Checks that segment 1 of each channel can be written with an incrementing pattern. Writes to all channels simultaneosly from zero address through to the end of memory then reads back, starting with channel 1.

6.2.3 Envelope Control Tests

Test name: RAMP
No. tests: 4
Options: F=n Filter cutoff frequncy.
Range 1-15, default=15

Test No.1 - "Ramp Preset"
Purpose: Tests ability to preset the envelope-shaping DAC

The envelope DAC is preset. The waveform DAC is provided with a steady data input of $FF while its reference voltage (the envelope) is cycled linearly between Ø and $FF. The ramp up/down counters are preset on every segment. A low frequncy triangle waveform should result at TP6 with 1.75V p-p amplitude. Terminate test and advance to the next by hitting the space bar.

Test No.2 - "Ramp Auto Run"
Purpose: The envelope of each segment may be ramped individually by the up/down ramp counters.

The ramp counters are allowed to free run until they reach Ø or $FF, whereupon the direction control bit is changed to ramp in the opposite direction. The result is a clipped triangle waveform, 1.75V p-p at TP6. Terminate test by hitting the space bar.

Test No.3 - "Force Ramp Up and Down"
Purpose: Checks ramp up/down override.

Ramp counters are allowed to ramp up and down as in test 2 but the direction control is overridden by the Force Ramp Up and Force Ramp Down controls. The same clipped triangle waveform should appear at TP6. Terminate test by hitting the space bar.

Test No.4 - "Ramp Zero Offset"
Purpose: Checks for noise or a DC offset from envelope DAC at zero output.

The ramp level is preset to zero. There should be negligible output (less than 300mV p-p) from the channel card at TP6.

6.2.4 Volume Control

Test name: VOL
No. tests: 2
Purpose: Checks volume control DAC.
Options: F=n Filter cutoff harmonic
Range 1-15, default 8
S=n Volume change speed
Range 1-127, default 1

The volume control DAC is the last stage in the audio processing system. With a DC reference (normally the envelope shaped and filtered waveform) volume data is cycled repetitively between zero and $FF. The cycle speed is controlled by the S option: 1 corresponds to maximum speed.

A triangle waveform of 2V p-p should be observed at TP6. Terminate the test by hitting the space bar.

Test No.2 - "Zero Offset Test"
Purpose: This test checks the zero offset of the fixed low-pass filter which precedes the volume DAC.

The latched volume level is set to zero. A trimpot should be available at the front of the channel card. If a buzzing sound occurs, accompanied by a small sawtooth waveform at TP6, adjust the trimpot until no buzzing is heard at max monitor volume. There should be no more than 300mV p-p of noise when the trimpot is set correctly. Terminate the test by pressing the space bar.

If no trimpot is on the board, refer to Field Change Notice 32.

6.2.5 Timer Tests

Test name: TIM
No. tests: 3

Test No.1 - "Timer Read/Write Latches"
Purpose: Checks ability to communicate with timer.

The 6840 timer contains 3 16-bit timer counters and 3 associated preset latches. First all timers are held in preset state and outputs enabled by writing $81 to the internal control registers. Then timer 1 preset latch is written with all numbers from 0 to $FFFF and its associated timer read back for verification after each write. (In the preset state each counter reflects the contents of its preset latch). The other two timers are then tested in the same way.
Each write/read is a double-byte transfer through the 8-bit buss.

Test No.2 - "Timer Internal Clock Timeout"
Purpose: Checks timeout action using internal clock.

Timers are programmed to be decremented from the internal clock and are all initialised to $FFFF. Timeout occurs when a timer decrements to zero. All three timers should timeout together. A software timer is used as a reference to detect early or missed timeouts. The 6840 status register is repetitively polled to check when timeout occurs.

Test No.3 - "Timer External Clock Timeout"
Purpose: Checks timeout action using external clock.

Clock timeout is verified using the external clock inputs. Using the same reference as test No.2, all three timers should timeout simultaneously.

6.2.6 Pitch and Octave Control

Test name: PIT
No. tests: 2

Test No.1 - "Octave Register"
Purpose: Checks accuracy of the octave control PIA.

With the pitch register held at max, octave register is cycled from 0 to 8. At each setting, a timer is used to time a waveform by presetting a segment count appropriate to that octave and selecting the RUN mode. If timeout occurs before the End of Sound is reached or if the timer value is greater than a certain tolerance when the end is reached, an error is generated. The timer is clocked by the internal clock .

Test No.2 - "Pitch Register Test"
Purpose: Checks accuracy of pitch control from PIA.

With the octave register held constant, the 10-bit pitch register is cycled from zero to maximum and and the same method is used to verify the waveform accessing frequency as in test No.1.

6.2.7 Interrupt Flags

Test name: FLG
No. tests: 4

Test No.1 "End of Sound Flag"
Purpose: Test the "last segment" flag.

An end-of-sound interrupt is generated when the waveform address counters reach maximum. To test this, the segment count is preset to the last segment ($7F), and 127 writes to waveform memory are executed. On each write, premature end-of-sound is checked for. The 128th write should then produce the interrupt.

Test No.2 "Terminal Ramp Flag"
Purpose: Test "clipping" flag.

Generated by zero or max count being reached by ramp counters With direction bit from set to "down", $80 is written to the ramp preset register. The status is then read to check for no terminal ramp flag. Then zero is written to the ramp preset and read again to check that the terminal ramp flag is present.

The direction bit is then cleared (ramp up) and $7F and $F written to the ramp preset to alternately clear and set the termina ramp flag.

Test No.3 - "Zero Crossing Flag"
Purpose: Test "middle of segment" flag.

Generated at the middle of every segment by waveform addres counter . The flag goes high when the within-segment byte coun reaches 64. The test asserts to clears the counter then does 63 write to waveform memory, checking each time that the flag is clear. On more write should then set the flag.

Test No.4 - "Zero Cross Interrupt Flag"
Purpose: Test "middle of last segment" flag.

Zero crossing interrupt occurs on first zero crossing after th segment timer timeout. The timer is programmed to be clocked by th internal clock. Until it times out, the zero-crossing interrupt i checked for no premature flag. After timeout the status is rea again to check that the zero-crossing flag has occurred. The addres counters are clocked at maximum pitch during the test.

## 6.3 Master Card Tests

The master card can be diagnosed using the program MAST.CM, run by typing

MAST<CR>

with the CMI diagnostics disc in drive Ø.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

Some MAST tests require at least one channel card to be installed in the CMI. These are indicated by the presence of a C option in the descriptions below.

### 6.3.1 Timer Tests

Test name: TIM
No. tests: 4

Test No.1 "Master Timer Read/Write Latches"
Purpose: Check ability to communicate with timer.

The 3 timers in the 6840 timer are put into the preset state and all numbers from zero to $FFFF written to the timer 1 latch. Each write is followed by a timer read for verification. Timers 2 and 3 are then tested in the same way.

Each write/read is a double byte transfer through the 8-bit buss.

Test No.2 "Master Timer Internal Clock Timeout"
Purpose: Check timeout operation under internal clock.

The timers are clocked by the internal clock. All three timers are initialised to $FFFF then started. A software timing loop is used as reference, and the timer status is continually polled for premature timeout. Timeout must occur within a certain tolerance before or after reference timeout. Clock outputs are enabled during the tests.

Test No.3 "Master Timer External Clock Timeout"
Purpose: Check timeout operation under external clock.

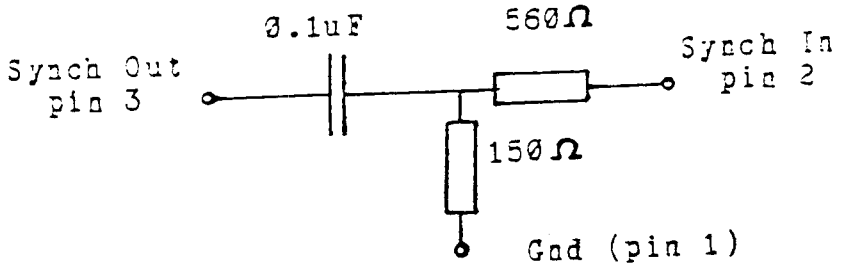
Timers are programmed as follows:-
Timer 2 Internal clock
Continuous operation
Initialised to 1
Output enabled

Timers 1&3 External clock (Timer 2 output)
Single shot
Initialised to $FFFF/2
Outputs enabled

The same reference is used to check that timers 1 and 3, being clocked by timer 2, times within tolerance.

Test No.4 "Master Synch In/Out"
Purpose: Checks click output and synch input circuits.

This is actually two tests run one after the other. Both require Synch In to be connected to Synch Out via an attenuator/ filter circuit in order to load the output. The circuit is illustrated below.




Synch Test Plug Circuit (3-pin Cannon)

The first test clocks the Synch In timer (timer 2) with a known frequency and checks its timeout against the software reference. During initialisation, timer 1 is checked to be working (i.e. that it can be made to time out). It is then programmed for internal clock and preset to run continuously at 250Hz with its output enabled. Timer 2 receives the sync input pulses and times out in single shot mode after 100 clocks (about 400mS). This timeout is verified against the software timer. Timer 3 is not used.

The second test sends a fixed number of pulses from timer 1 to timer 2 and checks that timer 2 receives the correct number. Timer 2 is set to internal clock and runs at 1000Hz. Timer 2 is initialised to $FFFF. The status register is polled for timer 1 timeouts and it is stoppped after 3000. Then timer 2's counter is read to check that it decremented to the correct number.

### 6.3.2 Master Pitch Register Test

Test name: PIT
No. tests: 1

Test No.1 "Master Pitch Register Test"
Purpose: Check for presence and accuracy of the master pitch reference signal MOSC.

This test requires a working channel card to be installed in the channel 1 slot. Each of the master pitch rate multipliers are tested separately by timing a number of segments and comparing it to a fixed value. The channel card is set at a fixed pitch, then the master pitch is preset through the master pitch register, starting with the lowest pitch. Timer 3 on the channel card is used to time the segments. The end-of-sound flag is cleared on the channel card then RUN mode selected and the timer started. The channel status is polled for the arrival of the end-of-scund and if it arrives outside a set tolerance from the timer 3 timecut, an error is generated.

This cycle is repeated for all master pitch settings.

a sufficient number of samples have been made and stored in channel
(& others if specified), sampling is stopped and the data in channel
read to check for a continuous rising ramp followed by a continuou
falling one. Each sample in the falling ramp is complemented first an
then checked as if it were a rising ramp.

Test No.2 "Analog to Digital Converter 30.2kHz"

This test is identical to test No. 1 except that a 30.2kH
sampling rate is used.

Error reports

If an error is occurs, a message is printed containing the erro
identification number, a description of the error, and an offse
indicating the address in the channel card memory where the error wa
detected. Some different error IDs give the same descriptive messag
and require further explanation:

Error #3 - "Difference too small"
Too many successive samples were identical. Test N=1 allow
only one repeated value, while N=2 allows two.

Error #6 - "Difference too large"
The difference between two sucessive samples was 2 or more
The comparison of samples is unsigned so this message may als
be generated when the difference is -1 (or any negativ
quantity), that is, when the ramp reverses its curren
direction for one or more samples.

Error #7 - "Difference too large"
Too many jumps of two were detected over the whole ramp. Test N=
allows up to 10 jumps of two but N=2 does not allow any.

Test name: ADCHK
No. tests: 2
Purpose: AD conversion test for debugging.
Options: C=n Channel number
Range=1-8, default 1 (always used)
R=n Audtype
Range 0-2, default 0

Test No.1 "AD Run Continuous 16kHz"
Test No.2 "AD Run Continuous 30.2kHz"

These tests are the same as the AD tests except that sampli
continues indefinitely to assist in debugging problems discovered
AD.

Test Name: DI
No. tests: 1
Purpose: AD conversion display.
Options: C=n Channel no.
Range 1-8, default 1

Test No.1 "Display Routine"

This simply sets up the specified channel to play back the sampled waveform last recorded by AD or ADCHK. Monitor it at TP6 or the mixed output. It should be a low frequency triangle. It is not necessary to do this except for debugging purposes as the software checks for the correct sampled data itself.

Test Name: DUMP
No. tests: 1
Purpose: For close examination of sampled data
Options: C=n Channel no.
Range 1-8, default 1
S=n Segment no.
Range Ø-127, default Ø

The contents of the specified channel and segment are printed on the screen in hexadecimal. Divide the offset printed by the error report by 128 to calculate which segment to display.

6.3.3.2 AD Tests Using Internal Analog Source

These tests are designed to check the analog to digital converter where a complete CMI is being tested without using the Analog Tester box.

Test Name: ADI
No. tests: 2
Purpose: Tests A-D conversion system using a known analog input, generated from one of the channel cards.
Options: C=n Channel no.
Range 1-8, default 1
(Channel 1 always used, plus others as specified).
R=n Audio board type
Range 0-2, default 0

Test No.1 "Analog to Digital Convertor 16kHz"
Test No.2 "Analog to Digital Convertor 30.2kHz"

Channel 1 must be available to provide the AD conversion clock to the master card. The other channels specified (or channel 1 by default) are loaded with a two-segment triangle wave to simulate the test waveform provided by the Analog Tester in the AD test. If testing a complete CMI, connect the output of the channel to be used as the analog source to the EXT ADC input as below and set the ADC selector to EXT ADC (this bypasses the master bandpass filter).

| | Pin |
|---|---|
| GND | 1 |
| Side A | 2 |
| Side B | 3 |

Channel Output Socket

| Pin | |
|---|---|
| 1 | Ext ADC RTN |
| 2 | |
| 3 | Ext ADC IN |

EXT ADC Socket

The R option is to allow for the high gain of early version audio boards (prior to revision 4A.1). If it is desired to update an old board, refer to Field Change Notice 23. The option determines the channel volume setting for playing the test waveform, as follows:

R=0 Test is first performed with volume setting for the old version audio board. The first conversion value is read and, if wrong, the volume is set for the lower gain new version audio board. The test is then repeated.

R=1 Test is performed with volume set for an old audio board only.

R=2 Test is performed with volume set for the new version audio board only.

Instead of storing the converted data in a channel card, it is written to a system RAM buffer. When 256 bytes have been read the values are checked as follows:

(1) All values must be increasing, but up to 2 successive values may be the same.
(2) There can be at most 1 missing code.

Test Name: DBI
No. Tests: 1
Purpose: Close examination of sampled data.

Test No.1 "Display Contents of Buffer"

Half of the contents of the 256-byte buffer in RAM, representing one side of the sampled waveform are printed on the screen.

Test Name: DII
No. Tests: 1
Purpose: Replay sampled waveform
OPtions: C=n Channel no.
Range 1-8, default 1

Test No.1 "Display Routine"

The contents of the RAM buffer are moved to the specified channel card memory and the channel set running until CNTRL ESC is typed. Monitor the waveform at TP6. It should be a low frequency triangle.

This test allows a quicker check of sampled data than DBI. Both display routines are only necessary for debugging as the ADI test itself checks if sampled data is correct.

Test Name: JAM
No. tests: 2

Test No.1 "P2 Jam and Unjam"
Purpose: Checks correct functioning of the processor 1 HALT circuit used by AD conversions.

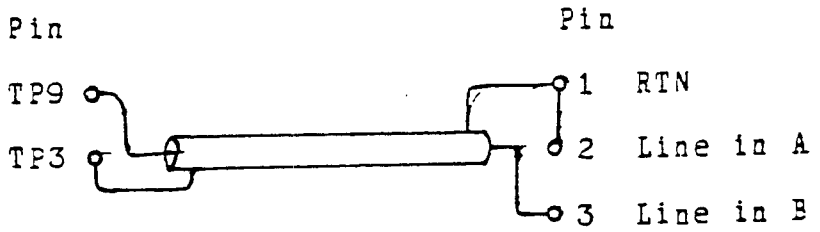
Test No.2 "P2 Jam Timeout"
Purpose: Tests the automatic processor 2 restart.

In the event of UNJAM never being accessed or a conversion never being completed, a hardware timeout is provided by a one-shot to restart P2. It must be possible to stop processor 2 for at least 200uS but no more than 1mS.is used as test No.1

6.3.4 Master Bandpass Filter Tests

Test Name: FILT
No. tests: 17
Purpose: Check characteristics of A-D converter input filter.
Options: C=n Channel number
Range 1-8, default 8

The specified channel is set up to provide an analog test waveform. A special cable with a plug matching the row of channel card test pins is used to take signal from channel crad TP9, the unfiltered analog output, to the LINE IN input of the audio board and thence to the master card Filter Input. Having made the connections as below, select LINE IN and INT ADC. Monitor the waveform at pin 3 of the SAMPLING FILTER OUT socket (pins 1 and 2 are GND) or TP10 of the master card.




Channel Card Test points LINE IN Socket

This test can also be performed using the Analog Tester box but the tester cannot gain access to the unfiltered channel output and uses the filtered output instead. This can indicate whether there is a major fault in the master filter but there is no point making accurate level measurements since the frequency responses of the channel card master card, MIC or LINE input amplifiers and the tester itself are all superimposed. Set the tester to FILT OUT ONLY.

The filter settings have the following effect:

| | |
|---|---|
| $X8-XF | LPF at minimum cutoff frequency |
| $X0 | LPF at maximum cutoff frequency |
| $0X | HPF at maximum cutoff frequency |
| $8X-FX | HPF at minimum cutoff frequency |

Tests 1 to 9 fix the HPF at minimum cutoff while ranging the LPF from maximum to minimum respectively (0-8). Tests 10-17 fix the LPF at maximum cutoff while ranging the HPF from minimum to maximum (7-0). Step through the tests using the space bar.

All tests fill 4 segments of the specified channel with a fundamental sine wave, followed by another 4 segments of the 3rd harmonic. Channel pitch is set for each filter setting to obtain a predetermined attenuation ratio between the two frequencies. Timer of the channel is set to loop around the 8 segments continuously and they are played through the analog bandpass filter at maximum vol and ramp settings.

Refer to Section 6.11 for expected waveforms.

## High-pass Filter 3dB Point

The 3dB point of the Master Filter at the lowest setting of the high-pass filter should occur at less than 20Hz. This can be tested by typing

FILT,N=9<CR>

This sets the filter at $F8, which is the lowest setting of both high pass and low pass filters. Instead of using the channel card as analogue input as above, connect a signal generator to the LINE IN socket (if single-ended, use side B, pin 3). Set input selector to LINE IN.

Monitor the master filter output at TP10 of the master card. With a line input of about 2.6V p-p at 500Hz, the filter output should peak at 10V p-p. Adjust frequency downwards until the filter output is 3dB down, i.e. 5V p-p. This frequency should be less than 20Hz.

See Section 11 for filter characteristics for all settings.

6.3.5 Video Ram Control

Test name: RAM
No. tests: 2
Purpose: Check ability to map VRAM in and out of processor address space.

Test No.1 "RAM VRAM Uniqueness Alternate Write"

The 16k of video RAM can be used as system RAM by processor 2 by clearing the CB2 bit of the PIA on the Master Card. This control is checked by first saving the contents of the screen (VRAM) in spare system RAM. Then the pattern $AA is written to $8000 (RAM), CB2 cleared to access VRAM, and the complement pattern ($55) written to VRAM $8000. This sequence is repeated for the entire 16k (with CB2 toggling after each write). Then the two blocks are alternately read from the beginning in the same way, to check for correct data in each block. Finally VRAM is restored to the original.

Test No.2 "RAM VRAM Uniqueness Alternate Read"

This is identical to test No.1 except that the pattern $55 is written to system RAM, and $AA to VRAM.

## 6.4.0 64K RAM Card Tests

### 6.4.1 MEMTST

A program for testing the 64K RAM card Q096 is MEMTST.CM which can be run by typing

MEMTST<CR>

with the CMI diagnostics disc in drive Ø.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

The program usually resides in block Ø (lowest 16K block) so tests which involve overwriting this area move it somewhere else first and bring it back afterwards.

Error messages will generally indicate the block where the error occurred. Block Ø is physically located on the Q-Ø96 board in the eight RAM chips of row F - furthest away from the edge connector. Blocks 1-3 are rows E, D, and C respectively.

Test name: 29
No. tests: 9

Test No.1 "Mapram"
Purpose: This tests the ability to select blocks one at a time without contention or overwriting.

With the test program running in block Ø, logical block 1 is mapped to physical block 1 (by writing the necessary data to mapram B3) and filled with 1's. Then logical block 1 is mapped to physical block 2 and filled with 2's. Similarly, physical block 3 is filled with 3's through logical block 1. That done, each physical block is selected in turn and read back for verification as logical block 1.

If no errors have occured, the contents of physical block Ø (including the program) are moved to physical block 3 and the test is repeated on blocks Ø-2.

Test No.2 "P1 Odd Up, P2 Even Up"
Test No.3 "P1 Odd Down, P2 Even Up"
Test No.4 "P1 Odd Down, P2 Even Down"
Test No.5 "P1 Odd Up, P2 Even Down"
Test No.6 "P1 Odd, P2 Even"
Test No.7 "P1 Even, P2 Odd"
Test No.8 "P1 All"
Test No.9 "P2 All"
Purpose: Test the ability of both processors to write and read every location in RAM independently without interfering with each other.

Each processor starts with a given data pattern "seed" and adds 29 (decimal), modulo 255, each time it writes. This creates a discontinuous but exhaustive data sequence which can be reproduced for verification.

"P1 Odd" means that processor 1 writes and reads all odd locations only, while "P2 Even" means processor 2 writes/reads all even locations only, and so on. Thus the data from each processor is interleaved in memory.

"P1 Up" means that processor 1 starts writing to the bottom of memory (lowest address) and goes up. Once it reaches the top, a reading phase is entered to verify the data pattern from the top of memory back to the bottom. Conversely "P2 down" means processor 2 starts writing at the top and works down, then reads back from bottom to top.

"All" means the specified processor writes and reads both even and odd locations.

Tests 6-9 cause one or both processors as specified to start at both ends, writing to the top and bottom alternately and working in towards the middle. When the middle is reached the reading phase begins, reading from the middle, out towards the top and bottom.

Test name: WA
No. tests: 2
Purpose: More RAM mapping tests

Test No.1 "Walking Address P2"
Test No.2 "Walking Address P1"

These test the RAM mapping by writing a "walking address" to the location specified by that address, testing one block at a time. First the block is filled with pseudo-random data. Then, starting at the bottom of the block the high order 8 bits of the current address is written to an even location then read back for verification. The low order address byte is written in the next location and verified. This is continued to the end of the block (incrementing the address by two for each high-order/low order write). Then the whole block is read again for verification from the beginning.

Test name: MAP
No. tests: 4

Test No.1 "Map Uniqueness"
Purpose: This tests the ability to select blocks one at a time without contention or overwriting.

This test is effectively identical to "29" No.1

Test No.2 "Card Deselect"
Purpose: By mapping any logical block to a physical block greater than 3 it must be possible to deselect the entire RAM card.

The program runs in block Ø as usual. Blocks 1-3 are filled with data $55. Then logical block 1 is mapped to "physical" blocks 4 to 7 in turn, reading the whole block for $55's which should never come up. This establishes that deselected blocks cannot be read.

To check they can't be written to, $AA is written to logical block 1 then physical blocks 3, 2 and 1 are checked to still contain $55.

Test No.3 "Write Protect"
Purpose: Blocks can be selected for reading only

Physical blocks 1-3 are filled with $55 and verified. Then each of these blocks are mapped in turn to processor 2 block 1 with the write-enable bit removed. The write-enable bit is the least significant bit of the mapping byte written to the mapram. For each mapping, logical block 1 is cleared. Then all three physical blocks are checked to still contain $55.

Test No.4 "Map-Processor Uniqueness"
Purpose: Processors can be mapped independently.

Physical block 1 is mapped to processor 2 block 1, and physical block 2 is mapped to process or 1 block 1. Processor 1 fills its logical block 1 with 1's, and simultareously, processor 2 fills its block 1 with 2's. Each processor then reads back its own block to verify for correct data.

## 6.4.2 MEMCH

A handy program for testing faulty 64K RAM cards is MEMCH.CM. However a good board is required to load it in the first place. With a good Q-Ø96 in the appropriate slot, type

MEMCH<CR>

with the CMI diagnostices disc in drive Ø. The program loads to $FFØØ, which is processor-unique static RAM on the processor control card. Halt both processors, swap the faulty RAM card in, and release the processors.

The program writes a binary count, verifying after each write, to location $1ØØ of each block.

6.5.0 Central Processor Control Module

Few diagnostics are available for testing this card (Q-032) since it is not possible to load the DOS and run a test without most of the card functioning correctly.

5.1 User PIA and Real Time Clock

The user PIA and real time clock is tested by the program DEBTST.CM, which may be run by typing

DEBTST<CR>

with the CMI diagnostics disc in drive 0.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

The PIA tests require a special test plug to be inserted in the user PIA socket (the one nearest the top of the board) which has the effect of connecting the A side of the PIA to the B side. Connections are as follows:

1 - 24, 2 - 25, 3 - 26,
5 - 22, 6 - 21, 7 - 20,
8 - 19, 9 - 18, 10 - 17,
11 - 16, 12 - 15.

Test Name: PIA
No. tests: 8

Test No.1 "PIA B/Send A/Receive"
Test No.2 "PIA A/Send B/Receive"
Purpose: With the test plug connecting the two sides of the PIA, A should be able to write to B and vice-versa.

Both tests check each side of the PIA individually first by defining the side as all bits inputs, changing them to outputs, then writing 0, $FF, $FE etc. down to 0 again to the data register and reading back to verify each write.

Test no.1 then sets side A as all inputs and side B as all outputs and writes all values from 0 decrementing back to 0 to side B, AND reading from side A. Test no.2 does the same in the opposite direction.

Test No.3 "CB2/Send CA2/Receive -ve"
Test No.4 "CB2/Send CA2/Receive +ve"
Test No.5 "CA2/Send CB2/Receive -ve"
Test No.6 "CA2/Send CB2/Receive +ve"
Purpose: Interrupt inputs/control outputs check.

The signal specified by "Send CX2" is configured as a control output whose state is determined by CRB-3 in the PIA control register. The other signal is configured as an interrupt input which will set the interrupt flag in the control register on an edge whose direction is indicated by the "Receive +ve or -ve".

The transmit end is first set to the state which will allow the wrong transition to cause an interrupt, (i.e. if the interrupt receiver is +ve edge triggered, the transmit end is set high) and the flag is checked as clear. Then the transmit state is toggled and checked again as still clear. A second toggle should trigger the interrupt flag.

The actual IRQ output is disabled during the test.

Test No.7 "CA1: RTC Input 16.3mS"
Test No.8 "CB1: RTC Input 16.3mS"
Purpose: Real time clock and CA1/CB1 operation

Interrupt input CB1 is always connected to a real time clock signal; inserting the test plug connects CA1 to it also.

During the test processor 1 is held in a tight loop to prevent it accidentally clearing the interrupt flag while processor 2 runs the test.

A long timeout loop is used first to check if the clock is working at all. The interrupt flag in the control reegister associated with CA1 or CB1 as specified is cleared then a polling loop entered to check if a new interrupt is received.

Immediately after the first "clock tick" is received, another counting/polling loop is entered to time when the next tick comes. When the second tick arrives the counter is checked to determine if clock is fast or slow. "Very slow" error message indicates that the most significant byte of the 16-bit counter was wrong.

## 6.6.Ø Light Pen Interface

### 6.1 CMILP

A quick check of the functions of the Light Pen Interface card C-148 is provided by the program CMILP.CM which may be run by typing

CMILP<CR>

with the CMI diagnostics disc in drive Ø. This test does not use the standard command interpreter.

The commands to CMILP are very simple:

I - Invert entire screen
C - Clear entire screen
Q - Quit

Just type the letter to initiate a command.

With the screen all "white" it should be possible to see the cursor field when the tip of the light pen is not touched, and draw single-dot "black" lines on the screen when it is touched. With the monitor adjusted to normal brightness the light pen sensitivity (a small screw under the rubber cap on the light pen body) should be adjusted so that the cursor is as small as possible but still distinct.

Check that it is possible to draw anywhere on the screen except the top two rows and the left most 8 columns. Try inverting the screen.

### 6.6.2 LPTST

For more careful diagnosis of a faulty board, use LPTST.CM run by typing

LPTST<CR>

with the CMI diagnostics disc in drive Ø.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

This section describes LPTST Version 1.3

### 6.6.2.1 Light Pen Timers

Test name: TIM
No. tests: 4

Test No.1 "Light Pen Timer Read/Write Latches"
Purpose: 6840 timer preset latches can be written to and the counters read.

Timers are put into preset state in which the counters always reflect the contents of the preset latches. Then each timer is write/read tested with all numbers from Ø to $FFFF. Each write/read is a 16-bit transfer through the 8-bit buss.

Test No. 2 "Light Pen Timer Internal Clock Timeout"
Purpose: Correct timeout from timers under internal clock

The internal clock is provided by the BCA signal. Timer outputs are enabled and latches preset to $FFFF. Then all three counters are released and their timeouts compared to a software status-polling (to sense timeout) timing reference loop.

Test No.3 "Light Pen Timer 2 External Clock"
Test No.4 "Light Pen Timer 3 External Clock"
Purpose: Timers under external clock

Timer 2 counts frames, thus gets a 20mS clock cycle. The test is not synchronised to the frame pulses so a +/-10mS jitter is permissible. The timer is preset to count 200 clocks (4 secs), then released and compared to the software reference with the required tolerance.

Timer 3 is clocked by processor 2 phase 2 (1MHz). It is preset to $FFFF then released and its timeout compared to the software reference.

Both timers run in single shot mode with outputs enabled.

### 6.6.2.2 Light Pen PIA

Test name: PIA
No. tests: 1

Test No.1 "PIA Test"
Purpose: You've got 3 guesses

Each side of the PIA is configured as all outputs then all numbers from zero backwards down to zero are written to the data latches and verified.

6.6.2.3 Processor Access Selection

"Test" name: SEL
Purpose: Allows user to specify which processor can access the videc RAM.
Options C=n CPU selection
Range 1-2, default 2

Used for special purpose testing only. Not applicable to C.M.I. which always uses processor 2 for VRAM operations.

6.6.2.4 Light Pen Drawing

Test name: LPEN
No. tests: 1

Test No.1 "Light Pen Drawing on Screen"
Purpose: Overall light pen operation, similar to CMILP.
Options: L=1 Range Ø-1, default 1
1 causes hit addresses to be written on the screen

S=s Range Ø-1, default 1
Ø inhibits resetting of the scroll reg.

Use LPEN the same way as CMILP. With hit address writing enabled, the location of each hit is written on the bottom line of the screen, both as X,Y coordianates and as an address in video ram. The line number is given first (zero at the top) followed by two bytes representing the location of the hit on that line. The first byte should always be Ø or 1 and represents the least significant bit of the 9-bit location (512 dots per line). The second byte is the upper 8 bits of the location. The VRAM ADRS is the absolute address of the hit in video RAM and is followed by a byte indicating which bit of that address was hit.

6.7.Ø Graphics System

A functional check of the Graphics Controller Q-Ø45 and 16K Graphics RAM Q-Ø25 can be run by typing

GRAPH3<CR>

with the CMI diagnostics disc in drive Ø. This test doesn't use the standard command interpreter.

GRAPH3 does not test the Q-Ø25 directly as MEMTST tests the Q-Ø96 memory. However, graphics RAM faults will generally be apparent from the screen display. A software test of the Q-Ø25, though not exhaustive is the RAM VRAM Uniqueness tests in MAST (see section 6.3.5).

Graph3 Commands:-
A single hex digit Ø-B calls one of 11 simple graphics drawing functions. Each command begins in the centre of the screen and draws out in the specified direction to the edge and wraps back around to the centre. Drawing may be started and stopped, speeded up and slowed down as below:

| Type | Effect |
|---|---|
| 1 | Horizontal line to the right |
| 2 | Horizontal line to the left |
| 3 | Single horizontal byte at the centre |
| 4 | Vertical line downwards (single dot, pattern $8Ø) |
| 5 | 45 degree diagonal down to the right |
| 6 | 45 degree diagonal down to the left |
| 7 | Heavy vertical column downwards (1 byte wide, pattern $FF) |
| 8 | Vertical line upwards, single dot wide |
| 9 | 45 degree diagonal up to right |
| A | 45 degree diagonal up to left |
| B | Heavy vertical column upwards ($FF) |
| S | Slower speed |
| I | Increase speed |
| P | Change write pattern |
| E | Halt |
| C | Clear screen |
| G | Go |

All drawing is done a byte at a time and except for command 3 which only writes a single byte, consists of writing repetitively to the appropriate Q-Ø45 auto increment/decrement register. The Q-Ø45 specification sheet contains a list of which locations perform these automatic functions. By default, the drawing "pattern" is $FF so that all lines are unbroken. By using the P command the drawing pattern can be used to create broken lines. This is handy for finding single-bit

errors (usually originating on the RAM card). The vertical line commands 4 and 8 mask off all but the most significant bit so any pattern without this bit won't draw anything for those commands.

GRAPH3 should be used to check the location of video information between the horizontal synch pulses. This can be controlled by the two trimpots at the front of the Q-Ø45 board. RV2 (upper trimpot) sets the horizontal width, and RV1 (lower) sets the horizontal position. Adjust these using the double diamond pattern formed by commands 5 and 6 or 9 and A. The pattern should be symmetrical and just touch the edges of the active video area of the screen.

## 6.8.? Floppy Disc Controller

As is the case for the processor control card, nothing much can run if the floppy disc controller doesn't work. However there are two little programs described here which, once loaded using a good floppy controller, can be of some use in debugging the faulty QFC-2 board.

### 6.8.1 FDCFIX

The program FDCFIX.CM is loaded by typing

FDCFIX<CR>

with the diagnostics disc in drive ? and a working QFC-2 installed. This loads the program to $9FEE and exits immediately back to the operating system. Halt both processors, and swap in the faulty board but DO NOT connect the 50-way ribbon cable to the disc drives. Release the processors and press the console interrupt to enter the monitor. Type

A??Ø;G

to run the program (no <CR> required, and no message is printed to indicate the program is running).
All it does is loop around, alternately writing and reading the DMA status registers at $FCEØ to $FCE7. No verification is performed.

### 6.8.2 FDCDMA

The program FDCDMA.CM is loaded by typing

FDCDMA<CR>

with the diagnostics disc in drive Ø and a working floppy controller installed. It loads to around $A1ØØ but immediately exits back to QDOS without running.

Its function is to exercise the DMA logic. To get a DRQ signal on the faulty board, remove the floppy controller chip and insert a link between pins 38 and 2 of the socket (for in-house use, there is a dummy chip for this purpose).Halt the processors and swap the faulty board in but DO NOT connect the 50-way ribbon to the disc drives. Press console interrupt to enter the monitor and type

A1Ø2;G

to jump to the program (no <CR> is required, and no message is generated to indicate the program is running). The program is simply a little loop which writes $Ø4 to the DMA register at $FCE6 indicating a DMA read command, then writes $Ø5 (any number would do) to $FCEØ to generate a WE signal and hence a DRQ. Note that this does not test the DRQ under a write command.

6.8.3 QFC-2 Alignment

Adustment of two separate pulse lengths is required in the data separator section of the floppy disc controller. The test signals are available at points TP1 and TP2 and adjusted by 10-turn pots VR1 and VR2 respectively, on the QFC-2 board. With a CRO set to .5uS/div and positive triggered, both signals should be high for 2.7uS when no data is being read from the disc (TP1 gets reset earlier by data pulses when the disc is being read).

6.9.8 Interrupt Tests - CMIINT

CMIINT.CM is a program for testing all the interrupt mechanisms in a complete CMI. It is run by typing

CMIINT<CR>

with the CMI diagnostics disc in drive 0. It does not use the standard command interpreter but has its own commands to set up and run interrupt tests.

Each interrupt has a predetermined priority such that if two or more interrupts arrived since the last interrupt service, the one with the highest priority gets serviced first.

The "level" of an interrupt is a number indicating its priority such that the highest priority interrupts have a level of zero, and the others are arranged in ascending order of level for decreasing priority. The interrupts which may be tested by CMIINT, the part of the system from which they originate, their levels and the processor which services each one, are as follows:

| Name | Origin | Level | Processor |
|---|---|---|---|
| CHANNEL 1 | Channel 1 timer | 12 | 1 |
| CHANNEL 2 | Channel 2 timer | 8 | 1 |
| CHANNEL 3 | Channel 3 timer | 13 | 1 |
| CHANNEL 4 | Channel 4 timer | 9 | 1 |
| CHANNEL 5 | Channel 5 timer | 14 | 1 |
| CHANNEL 6 | Channel 6 timer | 10 | 1 |
| CHANNEL 7 | Channel 7 timer | 15 | 1 |
| CHANNEL 8 | Channel 8 timer | 11 | 1 |
| TIMER 1 | Master Card timer | 1 | 1 |
| ACIA 1 | CPU Control Card ACIA | 0 | 1 |
| TICKL 1 | Interprocessor intrpt | 2 | 1 |
| TICKL 2 | Interprocessor intrpt | 2 | 2 |
| TIMER 2 | Light pen timer | 1 | 2 |
| DISK 1 | Floppy disc controller | 0 | 2 |

CMIINT Commands

RUN Run tests on all active interrupts. Both sequential test (one interrupt at a time) and simultaneous test (triggered simultaneously, arrival checked for correct priority) will be run unless the SEQ or SIM commands have been used (see below). Run will be aborted if error count is exceeded or if the user hits CNTRL ESC (break).

REPEAT n Sets the repeat count to n. The original value is printed. A repeat count of zero will continue indefinitely until aborted.

ERROR n Sets maximum error count for RUN. Default is 1.

CMDS Print a list of available commands.

LIST List all interrupts and their statuses.

HELP Print a summary of how to use the test

QU Return to QDOS

+ <interrupt or function>
Activate an interrupt or function

- <interrupt or function>
Deactivate an interrupt or function

The interrupts which may be activated or deactivated using the + or - commands are as in the above list: just type + or - followed by the interrupt name. The "+" is always optional, and the name by itself will activate that interrupt or function. The functions which may be controlled in this way are:

| | |
|---|---|
| P1 | Testing of all processor 1 interrupts |
| P2 | Testing of all processor 2 interrupts |
| ALL | (De)Activate all interrupts |
| LEVEL n | (Ie)Activate all interrupts of level n |
| SEQ | Sequential testing |
| SIM | Simultaneous testing |
| EMSG | Generation of error messages |
| DISPLAY | Listing of recorded interrupts on screen |

General_Procedure_of_Tests

Initially, all interrupts are "active", i.e., will be tested upon typing the RUN command. Tests can be activated or deactivated using the commands above. Each test begins with the processor interrupt mask set so that interrupts currently pending are ignored. The status registers associated with each active interrupt is read in order to clear pending interrupts. These status registers generally contain a flag which indicates an interrupt has been generated and at this point the flag should be clear. All active interrupts are tested first sequentially (one at a time) then simultaneously. In the latter case, all active tests are "triggered" then the processor interrupt mask cleared.

A delay loop sufficiently long for all triggered interrupts to arrive is entered. The PICU's should continue to interrupt the processors with the currently highest interrupt pending until all have been serviced. A separate service routine is executed for each interrupt which records in a little block of data set aside for each one, its position in the sequence of interrupts when it actually arrived, whether that interrupt has been serviced before, and whether the interrupt flag in the associated status register is set. Then the flag is cleared.

At the completion of the delay loop the data blocks of each interrupt is checked to ensure the active ones arrived in the correct order and that no unexpected interrupts occurred.

Error_Messages

If error reporting has not been suppressed by a "-EMSG" command, messages will be generated indicating the error type and the interrupt test which generated it. The types of errors detected are as follows:

(1) "High Priority Interrupt Occurred Too Late"
Generated when the interrupt just received has a priority level less than the maximum found so far.

(2) "Interrupt Late ? Due to Previous Error"

One or more interrupts may appear to be late when they actually occurred at the right time, but a previous high-level (low priority) interrupt was too early and set an erroneously high current maximum level. The early low priority interrupt will not have been detected. This message is generated when the interrupt just received is consistent with the immediately preceeding interrupt (i.e. has a greater level) but has a lower level than the current maximum. Refer to the diagram on the following page for a clearer explanation of this problem.

(3) "Missing Interrupt"
An interrupt wich was expected never arrived

(4) "Multiple Interrupt"
An interrupt appeared to occur more than once. Usually caused by the interrupt not being cleared successfully by the service routine.

(5) "Unexpected Interrupt"
An inactive interrupt occurred.

(6) "Flag Not Set"
The service routine found that its associated interrupt flag had not been raised.

6.10.2 Testing a Complete CMI - Chain Tests

The CHAIN command is a facility which allows many tests such as those described above to be run with the minimum amount of human intervention. To run a series of tests, the command

CHAIN <filename><;options>

is used, where <filename> is the name of a special chain file containing a list of tests to be performed, and <options> are various option described below which control the execution of the chain.

This section is a description of the standard chain files used for testing a complete CMI.

6.10.1 Digital System Tests

Chain test name: CMITEST or CMITEST1
Purpose : All functions of a CMI which can be tested directly under software control (i.e. no waveform observations required)

CMITEST1 is for systems with only 1 disc drive and omits tests requiring 2 drives.

CMITEST requires a scratch or another diagnostics disc in drive 1.

| Test progs run | Commands executed |
|---|---|
| CMIINT | -DISK, RUN |
| DEBTST | All commands |
| CMITST | MEM, PIT, FLG, TIM |
| MEMTST | All commands |
| LPTST | PIA, TIM |
| MAST | PIT, RAM, JAM, TIM, AD |

Also - BACKUP (CMITEST only)
CHECK;V
COPY (drive Ø to drive 1 in CMITEST, Ø to Ø in CMITEST1)

Options:

| | |
|---|---|
| C=n | Channels to be tested. Default is 1-8 |
| -T | Omit timer (TIM) test in MAST |
| -MAST | Omit MAST altogther |
| AD | Include A-D conversion tests in MAST |

Test runs continuously, but can be aborted by hitting <cntrl ESC>.

Examples:

=CHAIN TEST (Run all tests as described above)

=CHAIN TEST;C=4,-MAST (Run all tests except Master Card and only use Channel 4)

6.10.2 Channel Card Analogue Tests

Chain test name: FRV
Purpose: Analogue functions of channel cards.

| Test progs run | Commands Executed |
|---|---|
| CMITST only | FILT, RAMP, VOL |

Options: none

All channels are tested. Step through the tests with a press of the space bar. FILT, RAMP and VOL are called on each channel individually, then FILT N=1 is called repetitively starting with channel 1 and adding another channel each time the space bar is pressed. This tests the mixer on the audio card in the back of the CMI. The amplitude should increase each time another channel is mixed in.

Example:
=CHAIN FRV (No options allowed)

6.10.3 Comprehensive Analogue Test

Chain test name: ANALOG
To check: all analog functions of the CMI channel cards, master card, and audio card.

| Test progs run | Commands executed |
|---|---|
| CMITST | RAMP, FILT, VOL |
| MAST | FILT, SYNC, AD. |

Options:
M Cmit channel card tests

This test is most conveniently used with the Analog Tester box connected to the rear panel of the CMI as labelled. Some cables need to be arranged slightly differently from normal. To make the changes, eject the disc(s), and turn power off first.
(1) Keyboard Power cable, normally connected from the CMI to the Music Keyboard, should go to the analog tester.
(2) Alphanumeric keyboard, normally connected to the Music keyboard, should be connected directly to the CMI rear panel.

The test program gives operator prompts and is thus largely self-explanatory. The following is some background on the use and functions of the analog tester.

Connection to Oscilloscope

The analog tester brings out both sides of the balanced outputs from the channel cards. With the oscilloscope set on 1V/div, add CH1 and CH2 and trigger on CH1.

The chain tests call standard tests described in previous sections which specify waveform measurements at TP6 of the channel card. This is only one side of the balanced output so measurements made using the analog tester will be about twice the amplitude found on TP6. For example in CMITST test FILT, the low frequency amplitude should be 6.8V p-p.

Switch 1 Phase Position

The phase check is to ensure that the different channels are in phase with each other.

Switch 1 Normal Position

This provides the balanced outputs to the CRC as above.

Mixed Out Test

This is the same as used in the FRV chain tests where FILT,N=1 is called repetitively starting with channel 1 only and mixing another channel in with each press of the space bar. The

amplitude should increase with each new channel, reaching a maximum of 6.8V p-p. This tests the audio mixer board in the back of the CMI.

MIC/LINE switching in MASTer test

By means of software and the analog tester, the output of channel 8 is fed to the MIC and LINE inputs and one or the other is fed to the Master card via the MIC/LINE switch. Although these two levels are actually quite different, the signals from the analog tester are similar in magnitude but still distinguishable. A sinusoidal waveform followed by a heavily attenuated harmonic should be observed with a peak amplitude of 1.5V p-p for MIC and 1.3V p-p for LINE.

The SYNC test

No measurement is required: the software will inform you of a fault although there is a filtered square wave which can be observed and an audible tone whose volume can be controlled by the SYNC MONITOR pot.

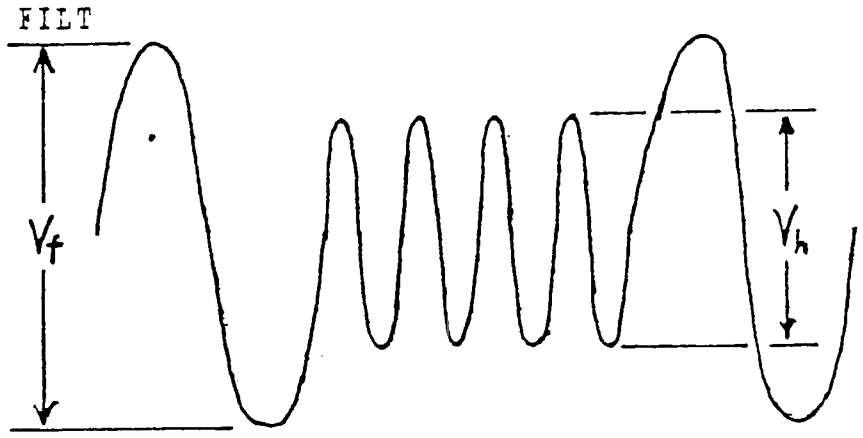
AD Test

This is also a software test only

## 6.11.0 Summary of Test Waveforms

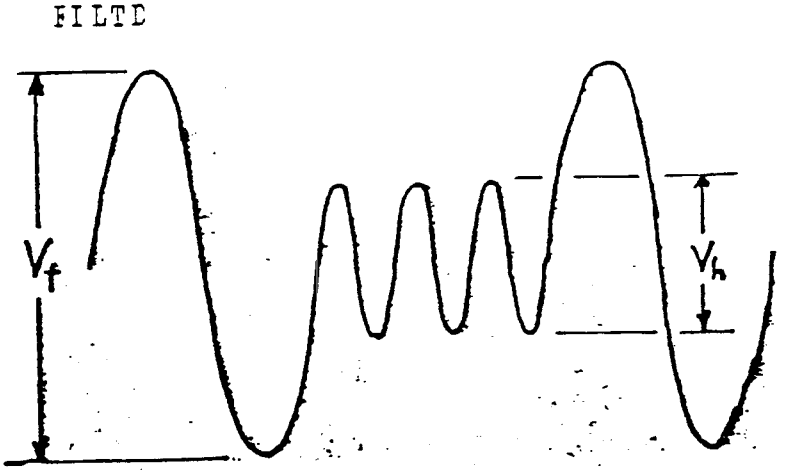
Measurement tolerances: refer to the introduction
(TP6) means measured at Test Point 6 of the Channel Card under test.
(AT) means measured using the Analog Tester, adding CRO channels.

### 6.11.1 CMITST




Vf = 3.4V p-p (TP6) for all tests
6.8V p-p (AT)

| Test N | 1 | 2 | 3 | 4-6 | 7-15 |
|---|---|---|---|---|---|
| Vh, V p-p (TP6) | 2.2 | 1.6 | 1.3 | 1.1 | 1.2 |
| Vh, V p-p (AT) | 4 | 3.5 | 3.3 | 3.0 | 3.2 |

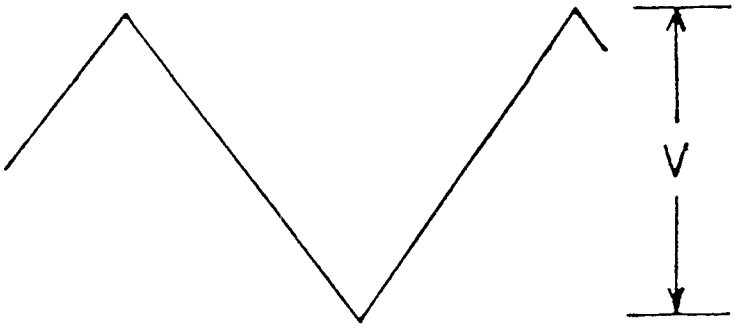



Levels depend on harmonic and filter settings. Levels for FILTD with default settings are as follows:

| Test N | 1 | 2 | 3 |
|---|---|---|---|
| Vf, V p-p (TP6) | 3.6 | 4.0 | 4.5 |
| Vh, V p-p (TP6) | 4.5 | <0.2 | <0.1 |

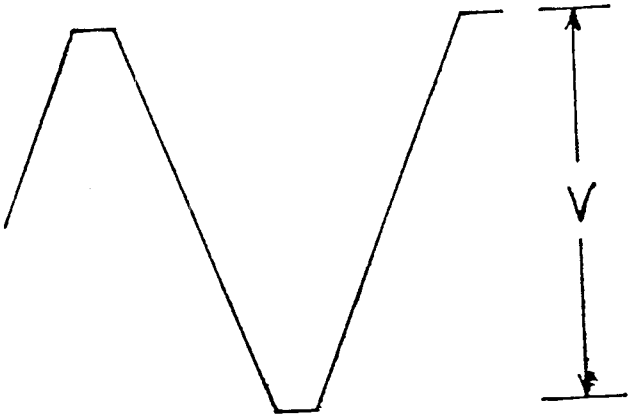
( "<" = less than)

RAMP, N=1 "Ramp Preset"



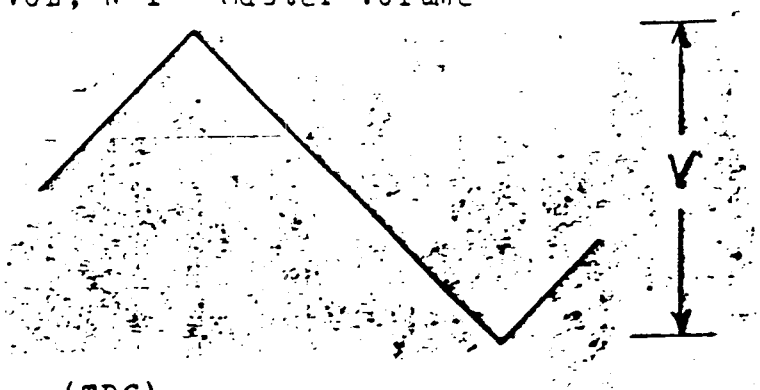

V = 2V p-p (TP6)
4V p-p (AT)

RAMP, N=2 "Ramp Auto Run"
N=3 "Force Ramp Up and Down"



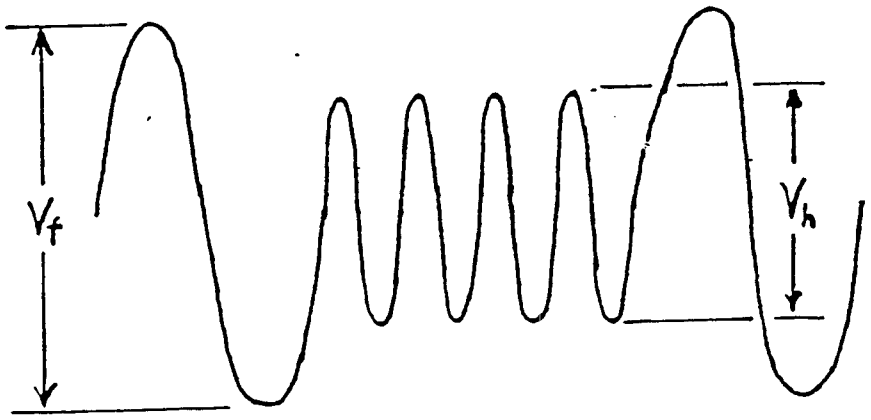

V = 2V p-p (TP6)
4V p-p (AT)

VOL, N=1 "Master Volume"




V = 2V p-p (TP6)
4V p-p (AT)

FILT




For N=1:
Vf = 4V p-p at FILT CUT
1.5V p-p for AT with CMI switched to MIC IN
1.3V p-p for AT " " LINE IN

N= 1 to 11, Filter Cutput:

| Test N | 1 | 2-5 | 6-7 | 8-10 | 11-17 |
|---|---|---|---|---|---|
| Vf, V p-p | 4 | 3.8 | 3.4 | 3.2 | 1.5 |
| Vh, V p-p | 2 | 2.2 | 2 | 2 | 3 |

## 7.0 SIGNAL LIST - MOTHERBOARD

All CMI modules, with the exception of the Audio, Front Panel a Power Supply modules, plug directly into 78 pin edge connecto mounted on the CMI motherboard PMB-01. This is in turn mounted on t rear of the CMI card cage. The motherboard is the means by which a logic signals and power supplies are routed between the plug- modules. This section specifies each of these signals for each modul starting from the left.

All modules are "double sided" so require two columns of pins each connector. "Side A" refers to the wiring side of the board whi corresponds to the left hand column of pins when viewed from the fro of the card cage. Conversely, "Side B" refers to the component side the board and connects to the right hand column of pins on the ed connector.

Pin numbers not included in the following lists are not used, a such pins are removed from the edge connectors before assembl Signals which are listed but have N/C marked as the source destination are those which have been connected to pins on the ed connector socket but have no connection leading to or from them on t motherboard.

Active-low signals are indicated by the name being overlined. A other signals are active-high. Where different names have been us for one signal going between various modules, the Signal Name colu contains the name for the module of the current section, and t alternative name is enclosed in brackets in the Source/Destinati column.

## 7.1 Master Card CMI-Ø2 - Slot 1

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 78-77 | +5V | Logic power supply | I/P | |
| 76 | ADINT | A/D conversion IRQ | C/P | QØ32 (IL62) |
| 75 | P2IR2 | Interprocessor intrpt (P2 level 2) | C/P | Q032 (IL22) |
| 74-67 | CHS7 - CHSØ | Channel select mask | O/P | All channels |
| 65 | RAMEN | System RAM enable | C/P | 64K RAM (AB2) |
| 64 | IRQSYN | ACIA IRQ (P1 level Ø) | I/P | QØ32 |
| 63 | VRAMEN | Graphics RAM enable | C/P | Grphcs cont. |
| 62 | ILS1 | PICU latch strobe | I/P | Processor |
| 61 | IA31 | PICU cascade | O/P | QØ32 (IA41) |
| 60-58 | IA21-IAØ1 | Interrupt vector address bits 1-3 | C/P | Processor |
| 57 | IRQ1 | Interrupt request to Processor 1 | O/P | Processor |
| 56 | XIRQ | P1 IRQ from QØ32 PICU | I/P | QØ32 (IRQ1) |
| 54 | HLT | Processor 2 halt for A/D conversion | C/P | Processor |
| 53 | SCAS | Channel memory column address strobe | O/P | All channels |
| 52 | SRAS | Channel memory row address strobe | C/P | All channels |
| 51 | SRA | Channel row address multiplex signal | C/P | All channels |
| 50 | SREF | Channel memory refresh cycle | O/P | All channels |
| 48 | MOSC | Master pitch oscillator | O/P | All channels |
| 47 | P1IR11 | P1 level 4 IRQ | I/P | N/C |
| 46 | P1IR1Ø | P1 level 3 IRQ | I/P | N/C |
| 44 | ADCLK | A/D convert clock | I/P | Channel 1 |
| 42 | SYRES | System reset | I/P | QØ32 |
| 40 | ALD1 | Processor 1's address on the buss (for VRAM enable) | I/P | Processor |
| 37 | RA | Row address mux signal | I/P | Processor |
| 36 | CA | Column address mux sig. | I/P | Processor |
| 34 | CAS | Column address strobe | I/P | Processor |
| 33-26 | IØ-I7 | Data Buss | Both | Processor |
| 25-10 | MAØ - MA15 | Address Buss | I/P | Proc, QFC2 |
| 9 | VMA | Valid Memory Address | I/P | Proc, QFC2 |
| 8 | R/W | Read/write | I/P | Proc, QFC2 |
| 7 | Key | Socket index key | | |
| 6 | +12V | +12V supply rail | | |
| 5,4 | +/-12VRTN | +/- 12V supply return rail (->GND) | | |
| 3 | -12V | -12V supply rail | | |
| 2,1 | GND | Ground rail | | |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 44-46 | GND | Ground rail | | |

## 7.2 Channel Card CMI-01 - Slots 3 to 10

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 78,77 | +5V | +5V Logic supply | | |
| 74 | CHSX | Ch. 7 select (Slot 10) | I/P | Master |
| 73 | CHSX | Ch. 6 select (Slot 9) | I/P | Master |
| 72 | CHSX | Ch. 5 select (Slot 8) | I/P | Master |
| 71 | CHSX | Ch. 4 select (Slot 7) | I/P | Master |
| 70 | CHSX | Ch. 3 select (Slot 6) | I/P | Master |
| 69 | CHSX | Ch. 2 select (Slot 5) | I/P | Master |
| 68 | CHSX | Ch. 1 select (Slot 4) | I/P | Master |
| 67 | CHSX | Ch. 0 select (Slot 3) | I/P | Master |
| 53 | SCAS | Channel memory column address strobe | I/P | Master |
| 52 | SRAS | Channel memory row address strobe | I/P | Master |
| 51 | SRA | Channel row address multiplex signal | I/P | Master |
| 50 | SREF | Channel memory refresh cycle | I/P | Master |
| 48 | MOSC | Master oscillator | I/P | Master |
| 44 | ADCLK | A/D convert clock | O/P (Ch.1 only) | Master |
| 42 | SYRES | System reset | I/P | Q032 |
| 37 | RA | Row address (timing) | I/P | Processor |
| 34 | CAS | Column address strobe | I/P | Processor |
| 33-26 | D0-D7 | Data Buss | Both | Processor |
| 25-21 | MA0 - MA4 | Address Buss | I/P | Proc, QFC2 |
| 8 | R/W | Read/write | I/P | Proc, QFC2 |
| 7 | Key | Socket index key | | |
| 6 | +12V | +12V supply rail | | |
| 3 | -12V | -12V supply rail | | |
| 2,1 | GND | Ground rail | | |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 74 | CHINTX | Ch. 7 IRQ (Slot 10 ONLY) | O/P | Q032 (IL31) |
| 73 | CHINTX | Ch. 6 IRQ (Slot 9 ONLY) | O/P | Q032 (IL71) |
| 72 | CHINTX | Ch. 5 IRQ (Slot 8 ONLY) | O/P | Q032 (IL21) |
| 71 | CHINTX | Ch. 4 IRQ (Slot 7 ONLY) | O/P | Q032 (IL61) |
| 70 | CHINTX | Ch. 3 IRQ (Slot 6 ONLY) | O/P | Q032 (IL11) |
| 69 | CHINTX | Ch. 2 IRQ (Slot 5 ONLY) | O/P | Q032 (IL51) |
| 68 | CHINTX | Ch. 1 IRQ (Slot 4 ONLY) | O/P | Q032 (IL01) |
| 67 | CHINTX | Ch. 0 IRQ (Slot 3 ONLY) | O/P | Q032 (IL41) |
| 44-46 | GND | Ground rail | | |

## 7.3 Analog Interface Card CMI-07 - Slot 11

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 78-77 | +5V | Logic power supply | I/P | |
| 54 | FCXX | I/O ports access | I/P | Q032 |
| 46 | AIRQ | AIC IRQ | C/P | N/C |
| 42 | SYRES | System reset | I/P | Q032 |
| 41 | ADD2 | P2 address on buss | I/P | Processor |
| 40 | ADD1 | P1 address on buss | I/P | Processor |
| 39 | P20/2 | P2 phase 2 reference | I/P | Processor |
| 37 | RA | Row address mux signal | I/P | Processor |
| 36 | CA | Column address mux sig. | I/P | Processor |
| 34 | CAS | Column address strobe | I/P | Processor |
| 35 | RAS | Row address stobe | | |
| 33-26 | D0-D7 | Data Buss | Both | Processor |
| 25-10 | MA0 - MA15 | Address Buss | I/P | Proc, QFC2 |
| 9 | VMA | Valid Memory Address | I/P | Proc, QFC2 |
| 8 | R/W | Read/write | I/P | Proc, QFC2 |
| 7 | Key | Socket index key | | |
| 6 | +12V | +12V supply rail | | |
| 5,4 | +/-12VRTN | +/- 12V supply return (-> GND) | | |
| 3 | -12V | -12V supply rail | | |
| 2,1 | GND | Ground rail | | |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 44-46 | GND | Ground rail | | |

## 7.4 Light Pen Interface Q148 - Slot 12

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 78-77 | +5V | Logic power supply | I/P | |
| 76 | GBIT | Graphics bit clock | I/P | Grphcs cont. (BITCLK) |
| 75 | INVRT | Video invert | C/P | Grphcs cont. (INV) |
| 74 | TVTBIT | Not used on CMI | I/P | N/C |
| 72 | TVTSYN | Not used on CMI | I/P | N/C |
| 68 | RINT | Light pen timer IRQ | O/P | Q032 (IL12) |
| 67 | PENINT | Light pen hit IRQ | O/P | Q032 (IL52) |
| 66 | TOUCHINT | Light pen touch IRQ | C/P | Q032 (IL42) |
| 61 | GR | Graphics sync reset | I/P | Grphcs cont. (RESET) |
| 42 | SYRES | System reset | I/P | Q032 |
| 39 | P20/2 | P2 phase 2 reference | I/P | Processor |
| 37 | RA | Row address (timing) | I/P | Processor |
| 36 | CA | Column address (timing) | I/P | Processor |
| 34 | CAS | Column address strobe | I/P | Processor |
| 33-26 | D0-D7 | Data Buss | Both | Processor |
| 25-10 | MA0 - MA15 | Address Buss | I/P | Proc, QFC2 |
| 9 | VMA | Valid Memory Address | I/P | Proc, QFC2 |
| 8 | R/W | Read/write | I/P | Proc, QFC2 |
| 7 | Key | Socket index key | | |
| 6 | +12V | +12V supply rail | | |
| 2,1 | GND | Ground rail | | |

Side B - no connections

## 7.6 Processor Control (Q032) Module Q-032 - Slot 16

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 78-77 | +5V | Logic power supply | I/P | |
| 76 | IL32 | P2 level 3 IRQ | I/P | N/C |
| 75 | IL22 | P2 level 2 IRQ | I/P | Master (P2IR2) |
| 74 | IL12 | P2 level 1 IRQ | I/P | LPI RINT |
| 73 | IL02 | P2 level 0 IRQ | I/P | QFC2-65 (N/C) |
| 72 | IL31 | P1 level 3 IRQ | I/P | Ch 7 CHINTX |
| 71 | IL21 | P1 level 2 IRQ | I/P | Ch 5 CHINTX |
| 70 | IL11 | P1 level 1 IRQ | I/P | Ch 3 CHINTX |
| 69 | IL01 | P1 level 0 IRQ | I/P | Ch 1 CHINTX |
| 68 | ILS2 | P2 PICU latch strobe | I/P | Processor |
| 67-64 | IA42-IA12 | P2 intrpt vector addr. | O/P | Processor |
| 63 | IRQ2 | P2 interrupt request | C/P | Processor |
| 62 | ILS1 | P1 PICU latch strobe | I/P | Processor |
| 61-58 | IA41-IA11 | P1 intrpt vector addr. | O/P | Processor |
| 57 | IRQ1 | P1 interrupt request | C/P | Master (XIRQ) |
| 56 | NMI2 | P2 NMI request | O/P | Processor |
| 55 | NMI1 | P1 NMI request | O/P | Processor |
| 54 | RES2 | P2 restart | C/P | Processor |
| 53 | HLT2 | P2 HALT | C/P | Processor |
| 52 | RES1 | P1 restart | O/P | Processor |
| 51 | RES2 | P2 restart | C/P | Processor |
| 50 | W2 | P2 halt acknowledge | I/P | Processor |
| 49 | W1 | P1 halt acknowledge | I/P | Processor |
| 48 | REF | Refresh cycle | C/P | 64K RAM |
| 46 | ACK1 | Refresh acknowledge | I/P | Processor |
| 45 | REQ1 | Refresh cycle request | O/P | Processor |
| 44 | ROMEN | Restart ROM enable | I/P | Processor |
| 42 | SYRES | System reset | O/P | All modules |
| 41 | ADD2 | P2 address on buss | I/P | Processor |
| 40 | ADD1 | P1 address on buss | I/P | Processor |
| 39 | REFC/2(2) | P2 phase 2 reference | I/P | Processor |
| 38 | REFO/2(1) | P1 phase 1 reference | I/P | Processor |
| 37 | RA | Row address mux signal | I/P | Processor |
| 36 | CA | Column address mux sig. | I/P | Processor |
| 34 | CAS | Column address strobe | I/P | Processor |
| 33-26 | I0-I7 | Data Buss | Both | Processor |
| 25-10 | MA7-MA15 | Address Buss | I/P | Proc, QFC2 |
| 9 | VMA | Valid Memory Address | I/P | Proc, QFC2 |
| 8 | R/W | Read/write | I/P | Proc, QFC2 (normally) |
| 7 | Key | Socket index key | O/P | all modules (during refre |
| 6 | +12V | +12V supply rail | | |
| 3 | -12V | -12V supply rail | | |
| 2,1 | GND | Ground rail | | |
| 25-19 | MA6-MA0 | Address Buss | I/P | Proc, QFC2 (normal |
| | | | O/P | All mods (during refr cyc |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 76 | IL72 | P2 level 7 IRQ | I/P | N/C |
| 75 | IL62 | P2 level 6 IRQ | I/P | Master (P2IR2) |
| 74 | IL52 | P2 level 5 IRQ | I/P | LPI RINT |
| 73 | IL42 | P2 level 4 IRQ | I/P | LPI TOUCHINT |
| 72 | IL71 | P1 level 7 IRQ | I/P | Ch 6 CHINTX |
| 71 | IL61 | P1 level 6 IRQ | I/P | Ch 4 CHINTX |
| 70 | IL51 | P1 level 5 IRQ | I/P | Ch 2 CHINTX |
| 69 | IL41 | P1 level 4 IRQ | I/P | Ch Ø CHINTX |
| 68 | IPQSYN | ACIA IRQ | C/P | Master |
| 67 | IRQPA | User PIA IRQ A | O/P | N/C |
| 66 | IRQPB | User PIA IRQ B | O/P | N/C |
| 65 | RAMINH | System RAM disable (enable QØ32 card) | C/P | 64K RAM (RAMEN) |
| 64 | FCXX | Mapram, I/O ports access | C/P | 64K RAM, AIC |
| 62,61 | | Current loop TX | O/P | |
| 44-46 | GND | Ground rail (N/C) | | |

7.7 Central Processor Module C-226 - Slot 17

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 78-77 | +5V | Logic power supply | I/P | |
| 68 | ILS2 | P2 PICU latch strobe | O/P | Q032 |
| 67-64 | IA42-IA12 | P2 intrpt vector addr. | I/P | Q032 |
| 63 | IRQ2 | P2 interrupt request | I/P | Q032 |
| 62 | ILS1 | P1 PICU latch strobe | O/P | Q032 |
| 61-58 | IA41-IA11 | P1 intrpt vector addr. | I/P | Q032 |
| 57 | IRQ1 | P1 interrupt request | I/P | Q032 |
| 56 | NMI2 | P2 NMI request | I/P | Q032 |
| 55 | NMI1 | P1 NMI request | I/P | Q032 |
| 54 | RES2 | P2 restart | I/P | Q032 |
| 53 | HLT2 | P2 HALT | I/P | Q032 |
| 52 | RES1 | P1 restart | I/P | Q032 |
| 51 | RES2 | P2 restart | I/P | Q032 |
| 50 | W2 | P2 in wait state (BA) | O/P | Q032 |
| 49 | W1 | P1 in wait state (BA) | O/P | Q032 |
| 48 | ACK2 | P2 DMA acknowledge | O/P | QFC2 |
| 47 | REQ2 | P2 DMA request | I/P | QFC2 |
| 46 | ACK1 | Refresh cycle grant | O/P | Q032 |
| 45 | REQ1 | Refresh cycle request | I/P | Q032 |
| 44 | ROMEN | Restart ROM enable | O/P | Q032 |
| 43 | CSC | Master proc. clock | O/P | N/C |
| 42 | SYRES | System reset | I/P | Q032 |
| 41 | ADD2 | P2 address on buss | O/P | All modules |
| 40 | ADD1 | P1 address on buss | O/P | All modules |
| 39 | REFO/2(2) | P2 phase 2 reference | O/P | All modules |
| 38 | REFO/2(1) | P1 phase 1 reference | O/P | All modules |
| 37 | RA | Row address mux signal | I/P | All modules |
| 36 | CA | Column address mux sig. | O/P | All modules |
| 35 | RAS | Row address strobe | O/P | All modules |
| 34 | CAS | Column address strobe | O/P | All modules |
| 33-26 | D0-D7 | Data Buss | Both | All modules |
| 25-10 | MA0 - MA15 | Address Buss | ~~I/P~~ O/P | All modules |
| 9 | VMA | Valid Memory Address | ~~I/P~~ O/P | All modules |
| 8 | R/W | Read/write | ~~I/P~~ O/P | All modules |
| 7 | Key | Socket index key | | |
| 6 | +12V | +12V supply rail | | |
| 2,1 | GND | Ground rail | | |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 44-46 | GND | Ground rail | | |

## 7.8 Floppy Disc Controller QFC-2 - Slot 18

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 78-77 | +5V | Logic power supply | I/P | |
| 71 | EDL | Erable Daisy Level (?) | O/P | QFC2 ETL |
| 70 | ETL | Enable This level | I/P | QFC2 EDL |
| 69 | ENL | Enable Next Level | O/P | N/C |
| 65 | | N/C | | Q032 IL02 |
| 63 | IRQD | Floppy Disc Cont. IRQ | O/P | N/C |
| 48 | ACK2 | DMA cycle grant | I/P | Processor |
| 47 | RDMA | DMA request | O/P | Processor (REQ2) |
| 42 | SYRES | System reset | I/P | Q032 |
| 41 | ADD2 | P2 address on buss | I/P | Processor |
| 39 | 2C/2 | P2 phase 2 reference | I/P | Processor |
| 36 | CA | Column address (timing) | I/P | Processor |
| 34 | CAS | Column address strobe | I/P | Processor |
| 33-26 | I0-I7 | Data Buss | Both | Processor |
| 25-10 | MA0 - MA15 | Address Buss | O/P | All modules |
| 9 | VMA | Valid Memory Address | O/P | All modules |
| 8 | R/W | Read/write | O/P | All modules |
| 7 | Key | Socket index key | | |
| 6 | +12V | +12V supply rail | | |
| 3 | -12V | -12V supply rail | | |
| 2,1 | GND | Ground rail | | |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 44-46 | GND | Ground rail | | |

## 7.9 Graphics Controller Q-045 - Slot 9

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 78-77 | +5V | Logic power supply | I/P | |
| 76 | BITCLK | Graphics dot clock | C/P | LPI (GBIT) |
| 75 | INV | Video invert | I/P | IPI (INVRT) |
| 74-67 | CSØ -CS7 | Graphics RAM bit mask | O/P | Grphcs RAM |
| 66 | GND | Ground via 44B-46B | | |
| 65 | ENBL | Graphics RAM enable | I/P | Master (VRAMEN) |
| 64 | GND | Ground via 44B-46B | | |
| 63 | EXRDY | External Ready | C/P | N/C |
| 61 | RESET | Graphics sync reset | O/P | LPI (GR) |
| 60 | GND | Ground via 44B-46B | | |
| 59 | BLN | Video not-blank signal | O/P | N/C |
| 58 | GND | Ground via 44B-46B | | |
| 57 | LINE | Horizontal sync | O/P | N/C |
| 56 | GND | Ground via 44B-46B | | |
| 55 | BDR | Video byte clock | O/P | N/C |
| 54 | GND | Ground via 44B-46B | | |
| 53 | BSOC | FIFO shift out clock | O/P | N/C |
| 51,49, 47,45 | D,C,B,A | Lower 4 bits of raster line counter | O/P | N/C |
| 52,50, 48,46,44 | GND | Ground via 44B-46B | | |
| 43 | INCA | FIFO shift in clock | O/P | N/C |
| 42 | SYRES | System reset | I/P | C032 |
| 41 | ADD2 | P2 address on buss | I/P | Processor |
| 40 | AID1 | P1 address on buss | I/P | Processor |
| 39 | O/22 | P2 phase 2 reference | I/P | Processor |
| 38 | C/21 | P1 phase 2 reference | I/P | Processor |
| 37 | RA | Row address (timing) | I/P | Processor |
| 36 | CA | Column address (timing) | I/P | Processor |
| 35 | RAS | Row address strobe | I/P | Processor |
| 33-26 | DØ-D7 | System Data Buss | Both | Processor |
| 25-10 | MA0 - MA15 | System Address Buss | I/P | Proc, QFC2 |
| 9 | VMA | Valid Memory Address | I/P | Proc, QFC2 |
| 8 | R/W | Read/write | I/P | Proc, QFC2 |
| 7 | Key | Socket index key | | |
| 6 | +12V | +12V supply rail | | |
| 3 | -12V | -12V supply rail | | |
| 2,1 | GND | Ground rail | | |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 44-46 | GND | Ground rail | | |
| 33-26 | RDØ-RD7 | VRAM Data buss | Both | Grphcs RAM (DØ-D7) |

| | | | | |
|---|---|---|---|---|
| 25-12 | VA0-VA13 | VRAM Address buss | C/P | Grphcs RAM (MA0-MA14) |
| 9 | VVMA | VRAM VMA | O/P | Grphcs RAM (VMA) |
| 8 | VRW | VRAM read/write | O/P | Grphcs RAM (R/W) |

## 7.10 16K Graphics RAM C-025 - Slot 20

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 78-77 | +5V | Logic power supply | I/P | |
| 75 | CS | Full byte enable | C/P | N/C |
| 74-67 | CS0 -CS7 | Read/write bit mask | I/P | Grphcs cont. |
| 65 | RAMINH | Graphics RAM disable | I/P | Tied high |
| 48 | REF | Refresh cycle | I/P | Tied high |
| 37 | RA | Row address mux signal | I/P | Processor |
| 36 | CA | Column address mux sig. | I/P | Processor |
| 35 | RAS | Row address strobe | I/P | Processor |
| 34 | CAS | Column address strobe | I/P | Processor |
| 33-26 | D0-D7 | VRAM data buss | Both | Grphcs cont. (RD0-RD7) |
| 25-12 | MA0-MA13 | VRAM Address buss | I/P | Grphcs cont. (VA0-VA14) |
| 11,10 | MA14,MA15 | VRAM Address M.S. 2 bits | I/P | Tied low |
| 9 | VMA | Valid Memory Address | I/P | Grphcs cont. (VVMA) |
| 8 | R/W | Read/write | I/P | Grphcs cont. (VRW) |
| 7 | Key | Socket index key | | |
| 6 | +12V | +12V supply rail | | |
| 5,4 | +/-12VRTN | +/- 12V supply return rail (->GND) | | |
| 3 | -12V | -12V supply rail | | |
| 2,1 | GND | Ground rail | | |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|---|---|---|---|---|
| 44-46 | GND | Ground rail | | |

## 8.0 SIGNAL LIST - EXTERNAL CONNECTIONS

### 8.1 A.C. Mains

A.C. Mains Neutral, Active and Ground.

### 8.2 Graphics Power

A.C. Mains supply to Graphics Terminal. Switched by key switch on mainframe. This supply is always the same as the local mains potential.

### 8.3 Graphics

Video signal to Graphics Terminal and Light Pen signals to mainframe.

Connector Type: Cannon 5-pin.

| | |
|---|---|
| Pin 1 | Lightpen Hit. T.T.L. level, asserted low. On oscilloscope, appears as a series of low-going pulses about 1uS wide, repeated every 20mS, when the pen is pointed at a bright area of the screen. (See fig 3a) |
| Pin 2 | Lightpen Signal Return. Ground for lightpen signal cables. |
| Pin 3 | Lightpen Touch. T.T.L. level, asserted low. Normally at approx +4 volts, goes low (less than 0.4 V) when the end of the lightpen touched. |
| Pin 4 | Video Return. Ground for Video signal cable. |
| Pin 5 | Composite Video. 1V P-P video signal to Groaphics display. Format is 625 lines, 50 Hz frame rate. (See fig 3b) |

Figure 3a LIGHTPEN HIT SIGNAL

Figure 3 b COMPOSITE VIDEO

## 8.4 Keyboard Power

Unregulated power supply to music keyboard (also indiectl
supplies alphanumeric keyboard).

Connector Type: Cannon 7-pin.

Pins 1,2 +10V Return. Return (ground) for +10V supply.

Pins 3,4 +10V Supply. Unregulated supply, +9 to +11 volts.

Pin 5 -20V Supply. Unregulated supply, -18 to -22 volts.

Pin 6 +20,-20 Return. Return (ground) for + and - 2
supplies.

Pin 7 +20V Supply. Unregulated supply, +18 to +22 volts.

## 8.5 Keyboard

Bi-directional serial data between mainframe and music keyboard
including "busy" flags in both directions. Power supply is als
carried by this cable, to power the alpha-numeric keyboard if i
is connected instead of the music keyboard.

Connector Type: 9 Pin "D-Mini"

Pin 1 +18 to 22 volts unregulated supply. This is not used b
the music keyboard.

Pin 2 DON1. Signal to enable transmission of data from th
keyboard. RS-232 levels. Enabled: >7 volts. Disabled <
7 volts. With nothing being transmitted from th
keyboard, this signal should be at approx. +10 volts
When keys are pressed or released a burst of -10 vol
pulses should be seen for between 2 and 1
milliseconds.

Pin 3 -18 to -22 volts unregulated supply. This is not use
by the music keyboard.

Pin 4 FLAG1. Signal to diasble transmission of data from th
mainframe to the keyboard. Signal is normally +1
volts.

Pin 5 SIGNAL RETURN. Ground for data paths.

Pin 6 IATA IN. Serial data from keyboard to mainframe. Forma
is RS-232. Normally at -10 volts. When a key is presse
or released a burst of +10 volt pulses lasting approx.
3 mS sholud be seen.

Pin 7 POWER RETURN. Return (Ground) for + and - supplies.

Pin 8 Not Connected.

Pin 9 DATA1. Serial data from mainframe to keyboard. Forma
is RS-232. Normally at -10 volts. For each characte
sent from the mainframe to the alpha-numeric display
burst of +10 volt pulses lasting approx. 1 mS should b
seen.

8.6 Printer

Serial data from mainframe to printer, "busy" flag from printe
to mainframe, plus "device on" signal used to switch on printe
in readiness to receive data.

Connector type: Cannon 5 pin.

Pin 1 Signal Ground.

Pin 2 Not Connected.

Pin 3 FLAG0. "Busy" flag from printer. RS-232 levels. <-
volts when printer ready, >+7 volts when printer busy.

Pin 4 DON0. "Device On" control from mainframe to printer
RS-232 level, >+7 volts to enable printer, <-7 volts t
diable printer. This signal is optional as som
printers do not require it.

Pin 5 DATA0. Serial data to printer. RS-232 levels, ASCI
format. Normally at -10 volts. For each character sen
from the mainframe to the printer a burst of +10 vol
pulses lasting approx. 1 mS should be seen.

8.7 Phones

Output for driving headphones. Monitors the MIXED LINE output
Internally, this output is taken from the MONITOR (speaker
output via a 100 ohm resistor.

Connector type: 1/4" (6.25 MM) stereo phono jack.

The following signal lists refer to connectors on the rear of th
C.M.I. Mainframe.

8.8 Monitor

Output for driving a monitor speaker. The internal monit amplifier will deliver a maximum of 20 watts R.M.S. into an 8 o speaker. Note that the Mainframe is fitted with a 1 amp speak fuse which will blow if the monitor amplifier is driven to fu output under load for more than a second.

Connector Type: Cannon 3 pin.

Pins 1,2 Ground

Pin 3 Active. With all channels producing a full-amplitu sinewave and the MONITOR control turned up to the poi of clipping, this output should be approx. 38 volts P- (with no load)

8.9 Channels 1-8

Individual channel outputs (balanced, 600 ohms impedance).

Connector type: Cannon 3 pin.

Pin 1 Ground

Pin 2 Output Cold. Anti-phase output, maximum level 3. volts P-P.

Pin 3 Output Hot. Maximum level 3.7 volts P-P.

8.10 Mixed Line Output

Mixed output of all eight channels (balanced, 600 ohm impedance).

Connector Type: Cannon 3-Pin

Pin 1 Ground

Pin 2 Output Cold. Anti-phase output, maximum level 3. volts P-P.

Pin 3 Output Hot. Maximum level 3.7 volts P-P.

8.11 Sync

Synchronising input and output, for use with Music Composition Language (Page C) or Keyboard Sequencer (Page 9). This connector serves as both an input and ouput.

Connector type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 Sync Input. Pulses or tone of 1 to 20 volts P-P Waveform unimportant. Frequency range 2 Hz to 5 kHz Impedance 10 K ohms.

Pin 3 Click Output. Periodic pulse, rate controlled by Page 9 Sequencer or M.C.L. (Page C). Waveform is a spike of approx. 5 volts peak, approx. 5 mS wide, alternately positive and negative going.

8.12 Filter Out

Output of the bandpass filter used by the Analogue to Digital converter. It is designed to enable the operator to monitor the effect of various bandpass filter settings.

Connector type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 GROUND

Pin 3 OUTPUT. Amplitude for full-scale conversion is 10 volt P-P. Source impedance 600 ohms.

8.13 Mic In

Balanced, 600 ohms input suitable for high output dynamic or condenser microphones. When the MIC/LINE switch is in the MIC position, this input is fed to the Analogue to Digital converter.

Connector Type: Cannon 3-pin

Pin 1 GROUND

Pin 2 INPUT A

Pin 3 INPUT B

8.14 Line In

Balanced, 600 ohm line level input. This input is connected t
the Analogue to Digital converter when the MIC/LINE switch is i
the LINE position.

Connector Type: Cannon 3-pin

Pin 1 GROUND

Pin 2 INPUT A. Amplitude of 1.4 volts P-P required for ful
scale conversion.

Pin 3 INPUT B. Amplitude of 1.4 volts P-P required for ful
scale conversion.

8.15 ADC DIRECT

Direct input to the Analogue to Digital converter when the AD
DIRECT/ MIC LINE switch is in the ADC DIRECT position. Becaus
this input is Direct Coupled, any D.C. offset on this input wil
result in a D.C. shift of a sound sample.

Connector Type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 GROUND

Pin 3 INPUT. Amplitude for full scale conversion is 10 volt
P-P.

9.0 REMOVE/REPLACE PROCEDURES

9.1 CIRCUIT BOARD REMOVE/REPLACE

9.2 DISK DRIVE REMOVE/REPLACE

9.3 REAR PANEL REMOVE/REPLACE

9.4 AUDIO BOARD CMI-04 REMOVE/REPLACE

9.5 FAN ASSEMBLY REMOVE/REPLACE

9.6 MOTHERBOARD CMI-05 REMOVE/REPLACE

9.7 POWER SUPPLY REGULATOR REMOVE/REPLACE

9.8 D.C. SUPPLY REMOVE/REPLACE

9.9 CARD CAGE REMOVE/REPLACE

## 10.0 REPAIR PROCEDURE

Having identified the faulty item, the following procedure is recommended:

1) Circuit Card Faults. Replace with spare card and return to Fairlight for repair.

2) Power Supply Faults. Repair following remove/replace instructions, functional description and related drawings.

3) Disk Drive Faults. Replace with spare drive. If fault is minor (e.g. alignment) adjust as per Fairlight Disk Drive Service Manual. In case of other fault, return to qualified Y.E. Data service centre or Fairlight for repair.

4) Electrical Faults. Repair by referring to appropriate wiring diagrams. Certain cable assemblies are available as spare parts from Fairlight (e.g. disk drive 50-way ribbon).

5) Mechanical Faults. Mechanical damage caused by wear and tear or accidental damage should be rectified by replacing the damaged item. Refer to section 16 (Exploded Views) below to identify the required part(s) for ordering.

@CT

## 11.0 PREVENTATIVE MAINTENANCE

The following procedures should be carried out every 1000 hours o operation.

1) Revove the top cover of the Mainframe and clean the mesh above th fans using a vacuum cleaner.

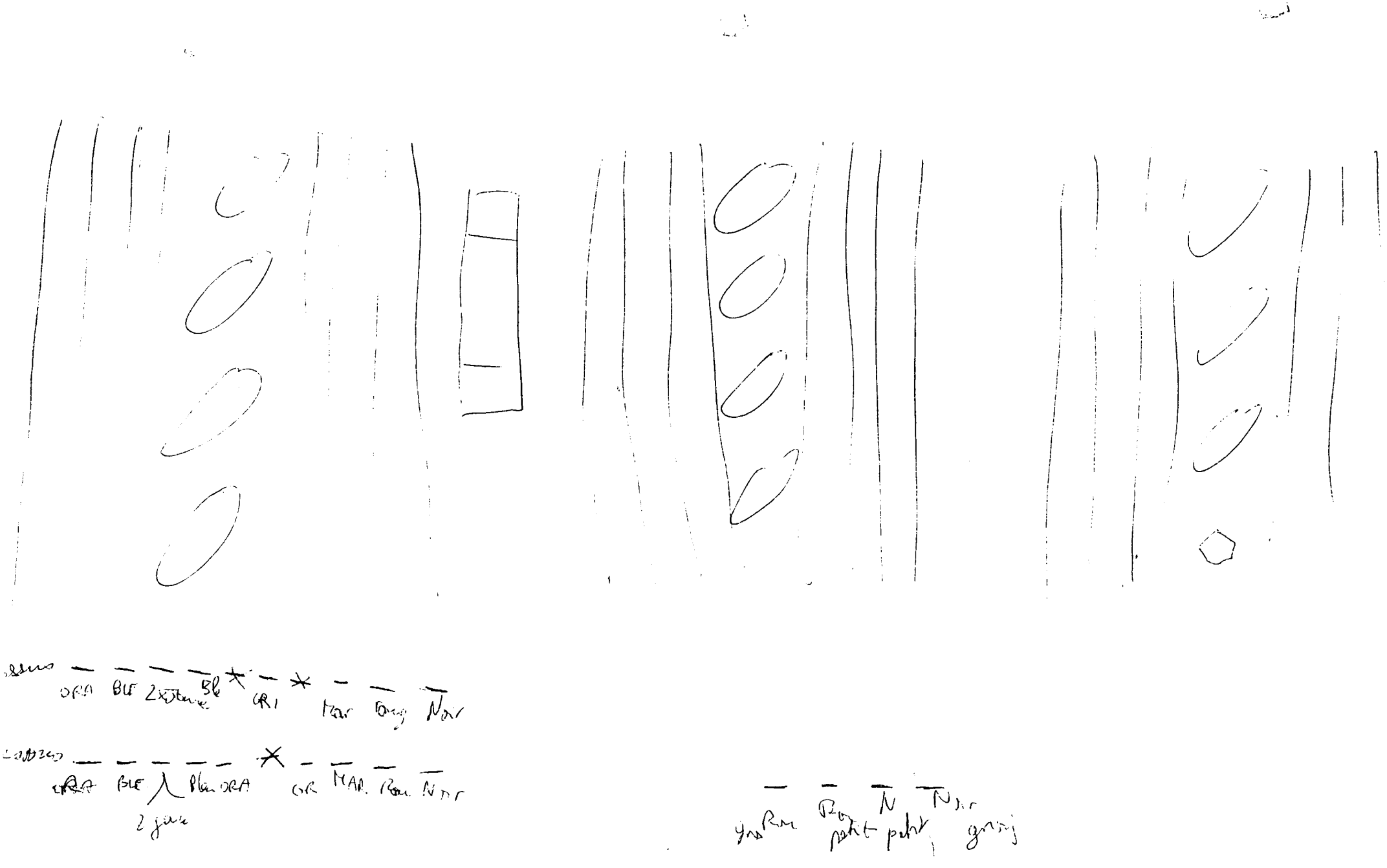
2) Unplug each circuit board, remove dust deposits from components an clean edge connector fingers using a soft cloth and a no-residu solvent such as freon. Check that the polarising key is properl installed in position 7 of each edge connector socket befor replacing the cards.

3) Check all cables for signs of mechanical damage e.g. fraying Ensure that all connectors are in good condition, especially mas termination ribbon connectors.

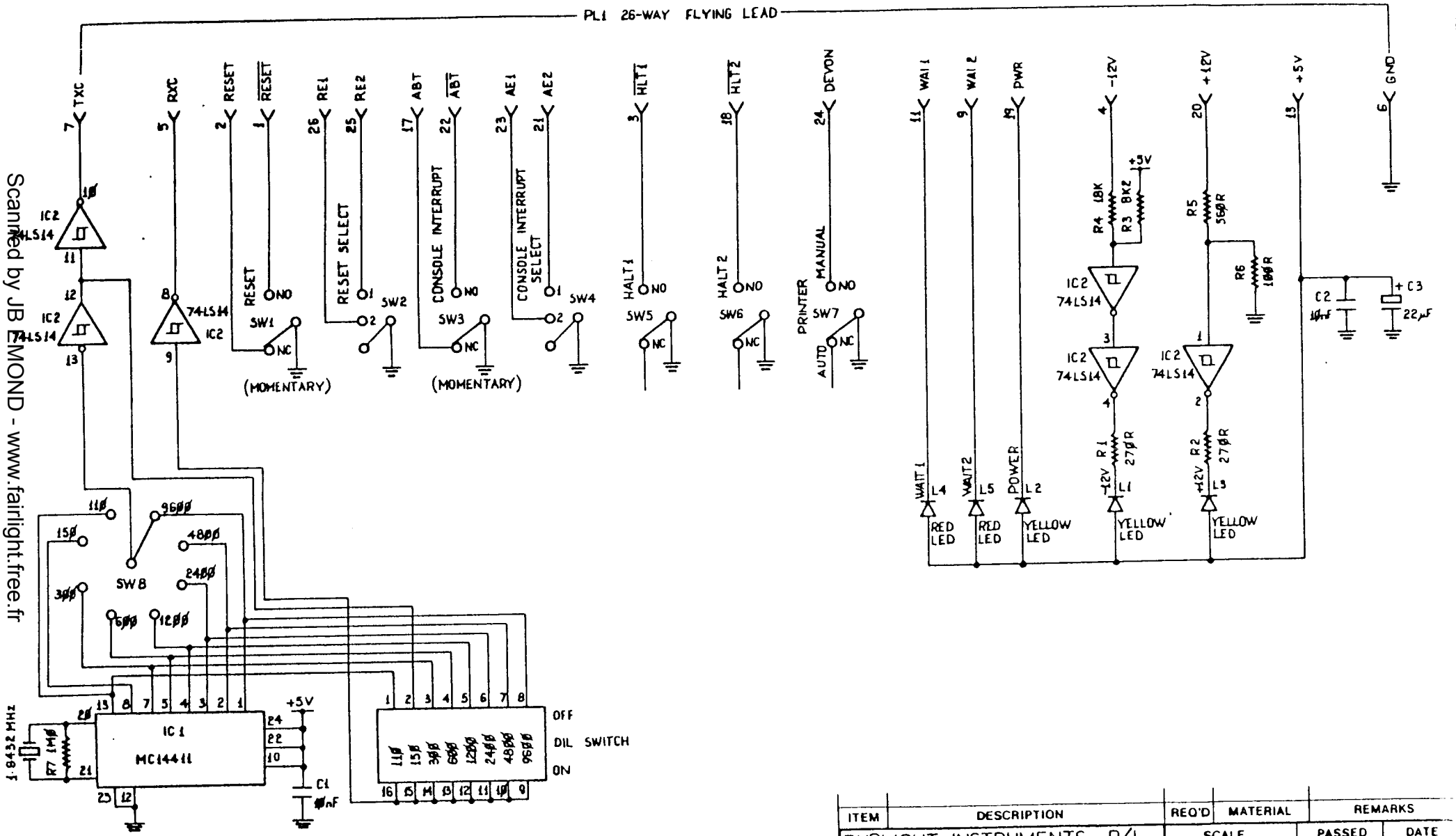
4) Check for mechanical damage such as bent panels or loose screws.

5) Check out all electronic functions using the Chain Tests (Refer t section 6 above).

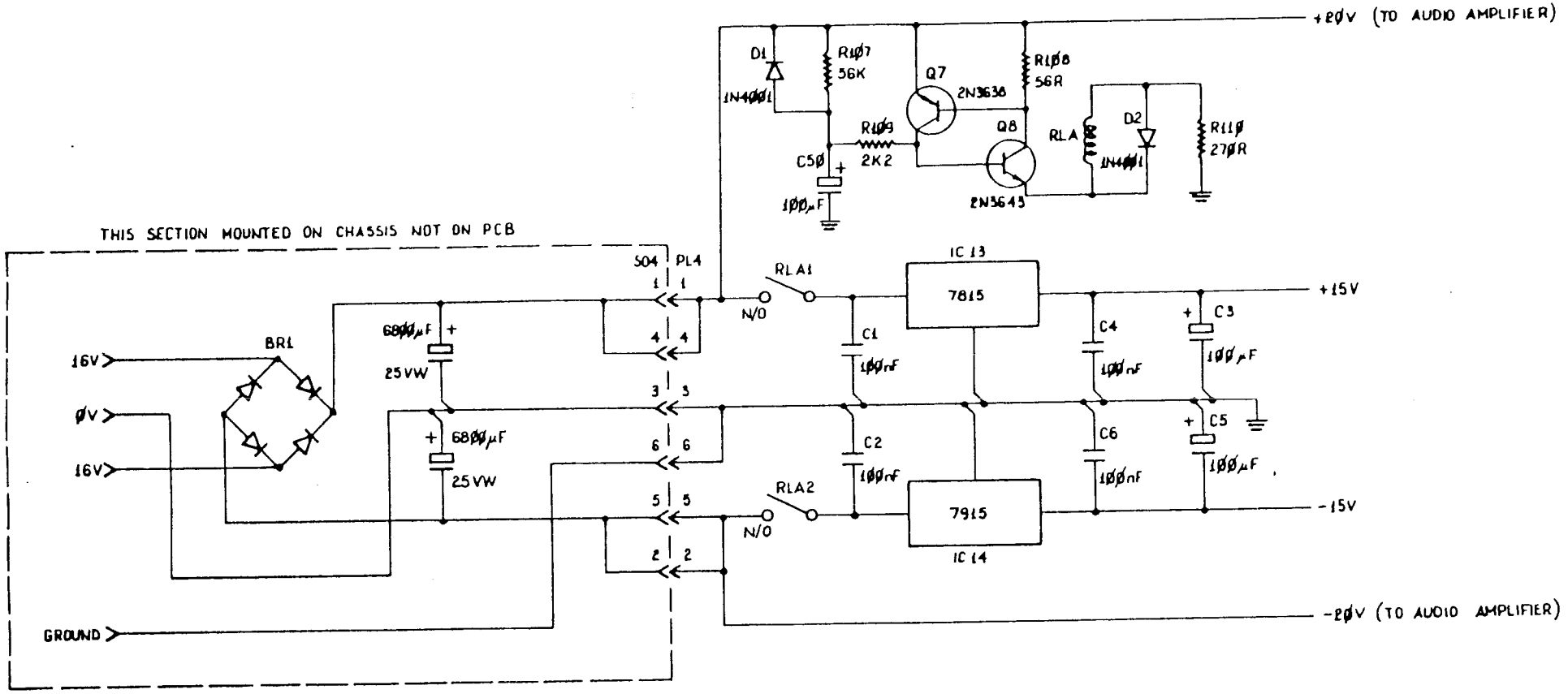
6) Check disk drives as per Disk Drive Maintenance Manual.



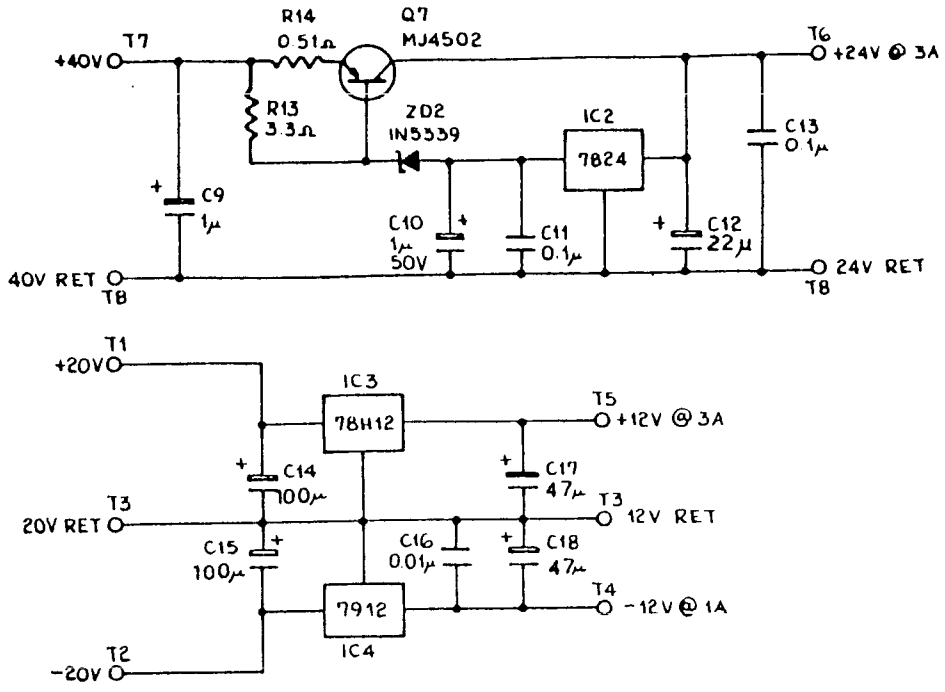
CARTE ALIMENTATION 2X



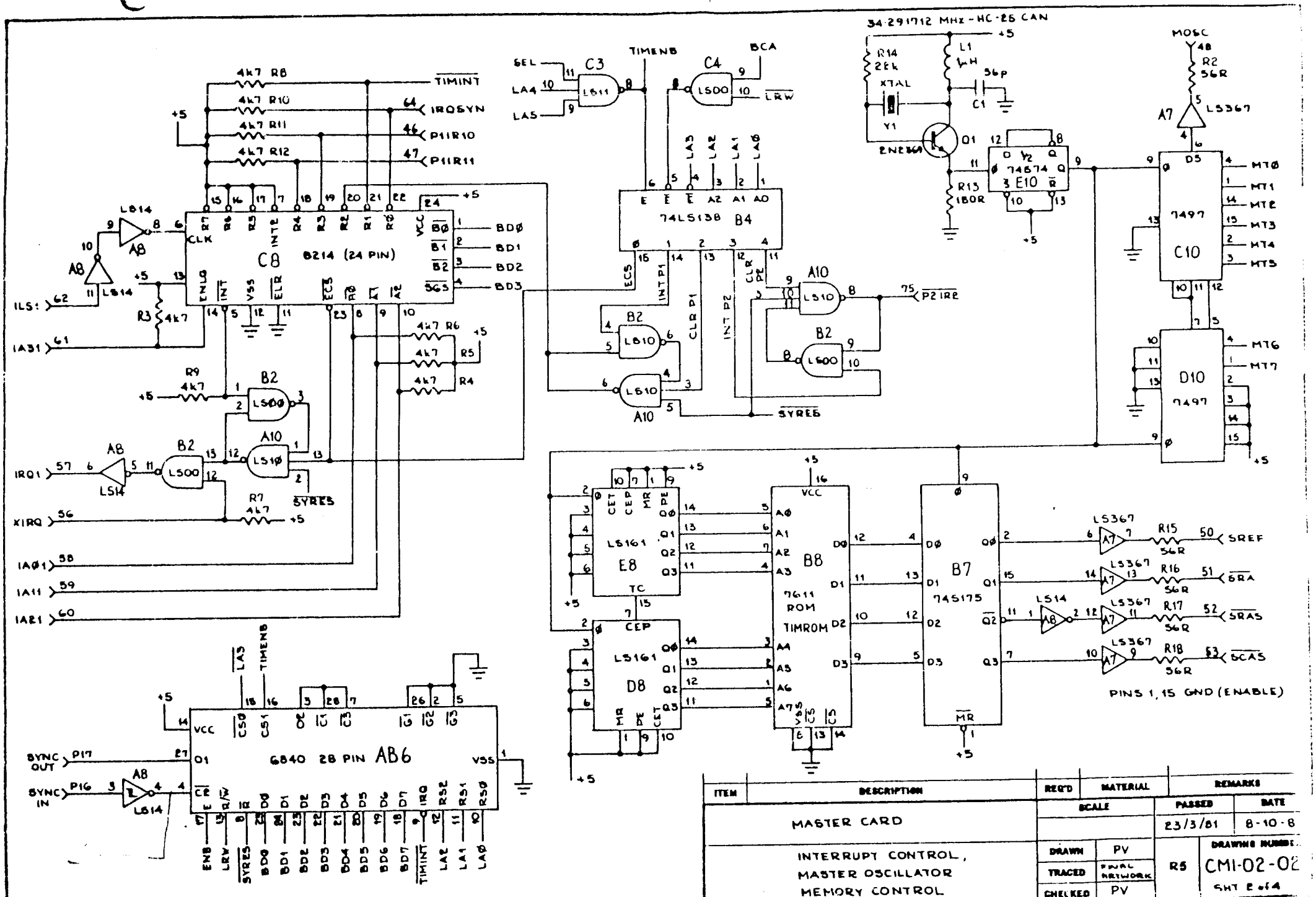

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>15 BOUNDARY ST RUSHCUTTERS BAY 2011<br>(02) 335222 | | SCALE | | PASSED / DATE<br>1/7/1982 / 9/11/197[illegible] |
| CENTRAL PROCESSING SYSTEM<br>CONTROL & DISPLAY PANEL<br>Sheet 1 of 1 | DRAWN A.G.F.<br>TRACED B.P.L.<br>CHECKED P.V. | | | DRAWING NUM:<br>Q036-01 |



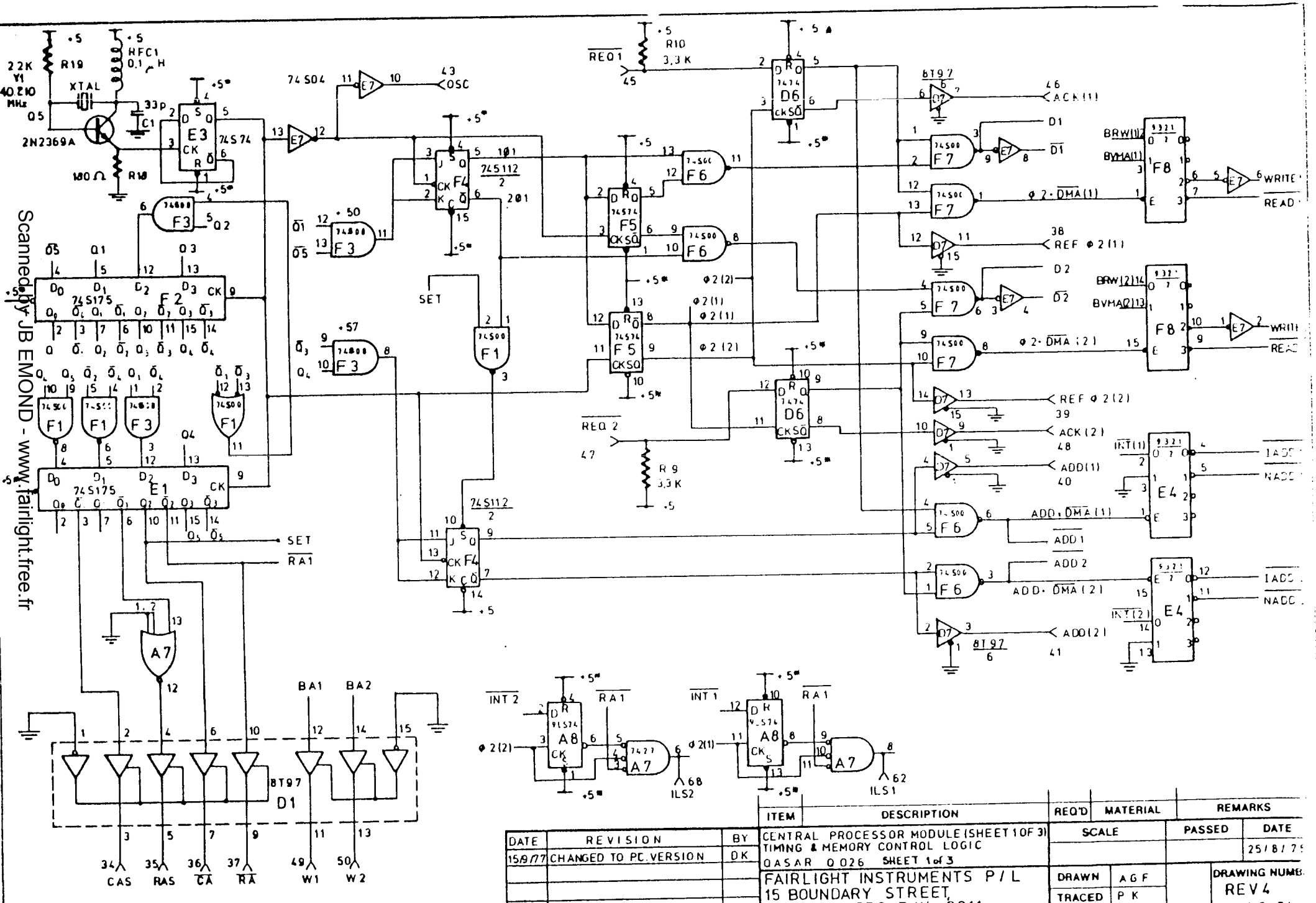

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>15 BOUNDARY ST RUSHCUTTERS BAY 2011<br>(02) 335222 | | SCALE | | PASSED 1/7/1982 DATE 11/04/19? |
| CMI AUDIO MODULE REV 4A2<br>POWER SUPPLY | | DRAWN P.V<br>TRACED B.P.L. | | DRAWING NUMB<br>CMI-04-0? |




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | C.M.I | SCALE | | PASSED / DATE: 3/2/81 |
| | POWER SUPPLY ASSEMBLY<br>±12V, 24V REGULATORS<br>SHEET 2 of 2 | DRAWN: DK<br>TRACED: MTB<br>CHECKED: PV | | DRAWING NUMBER: QPSA-Ø2 |




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | MASTER CARD | SCALE | | PASSED 23/3/81 DATE 8-10-8 |
| | INTERRUPT CONTROL, MASTER OSCILLATOR MEMORY CONTROL | DRAWN PV; TRACED; CHECKED PV; FINAL ARTWORK | R5 | DRAWING NUMBER CMI-02-02 SHT 2 of 4 |





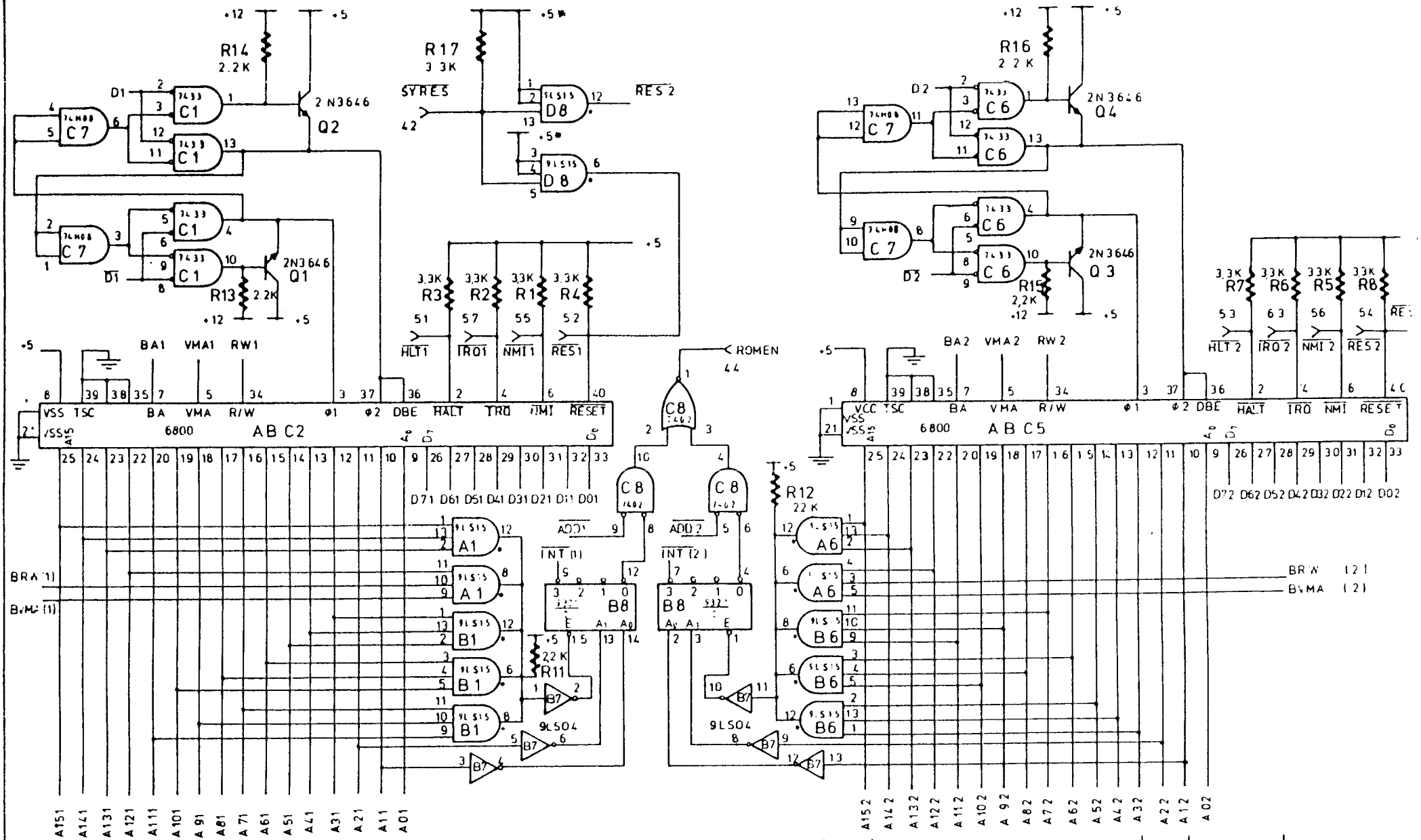

| DATE | REVISION | BY |
|---|---|---|
| 15/9/77 | CHANGED TO PC VERSION | DK |

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | CENTRAL PROCESSOR MODULE (SHEET 1 OF 3)<br>TIMING & MEMORY CONTROL LOGIC<br>OASAR 0026 SHEET 1 of 3 | SCALE | | PASSED / DATE: 25/8/7 |

FAIRLIGHT INSTRUMENTS P/L
15 BOUNDARY STREET,

| | |
|---|---|
| DRAWN | A G F |
| TRACED | P K |

DRAWING NUMB
REV 4

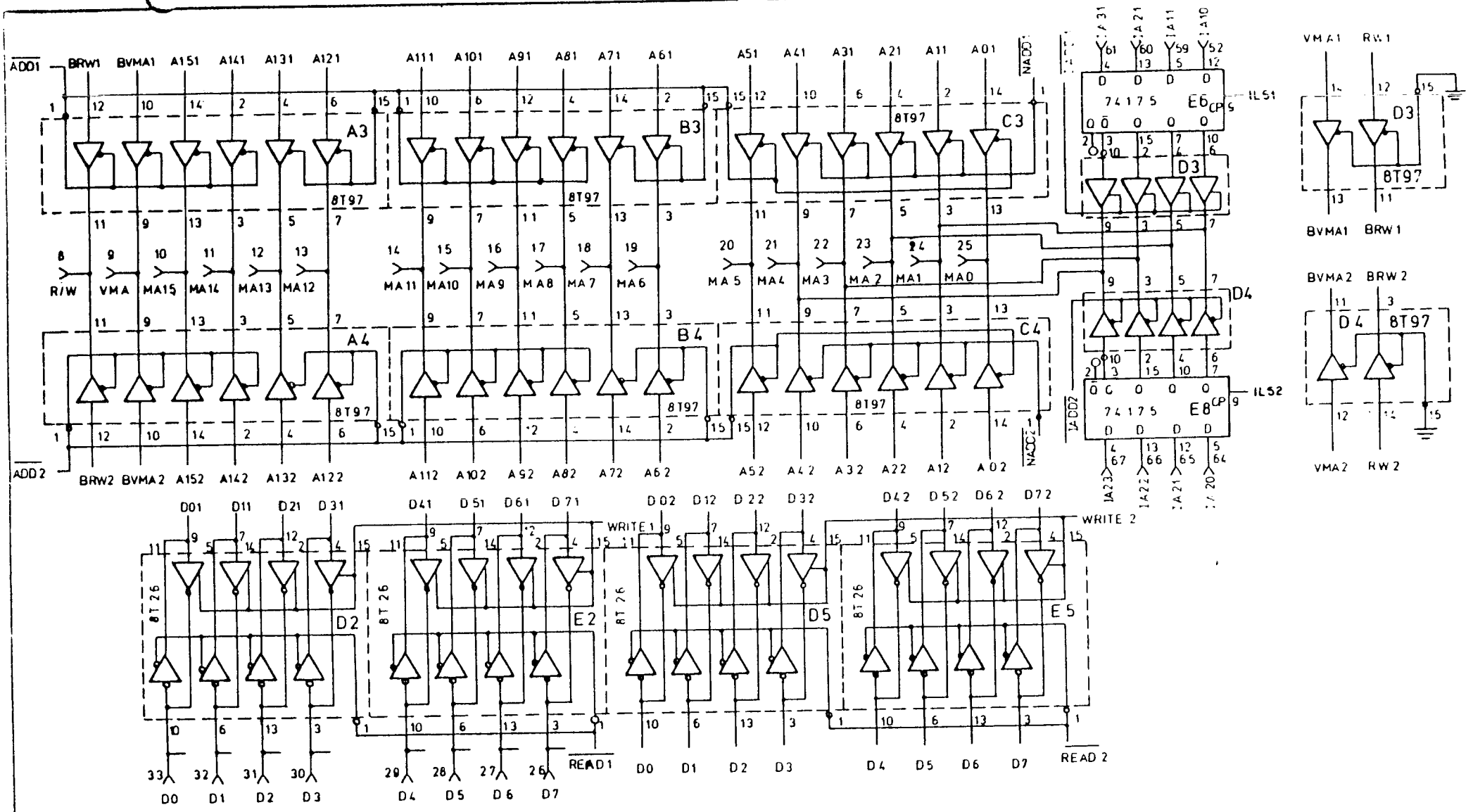


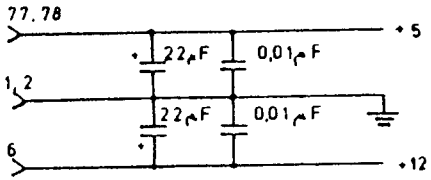

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | CENTRAL PROCESSOR MODULE SHEET(2 OF 3) CLOCK DRIVERS, CPU'S & DECODERS | SCALE | | PASSED / DATE |
| | Q A S A R 0 0 2 6 SHEET 2 of 3 | | | 27/8/7 |

| DATE | REVISION | BY |
|---|---|---|
| 15/9/77 | CHANGE TO PC VERSION | D K |

FAIRLIGHT INSTRUMENTS P / L
15 BOUNDARY STREET

| | |
|---|---|
| DRAWN | A G E |
| TRACED | P K |
| DRAWING NUM | Q Φ 26-02 |




BYPASS CAPS DISTRIBUTED AS REQUIRED AROUND BOARD

| DATE | REVISION | BY |
|---|---|---|
| 15977 | CHANGED TO PC VERSION | D K |
| 18 779 | INTERRUPT ADDRESS LATCHES | P V |
| 15980 | PC VERSION REV. 4 | C T |
| 29120 | INT. ADDRESS OPTION | P V |

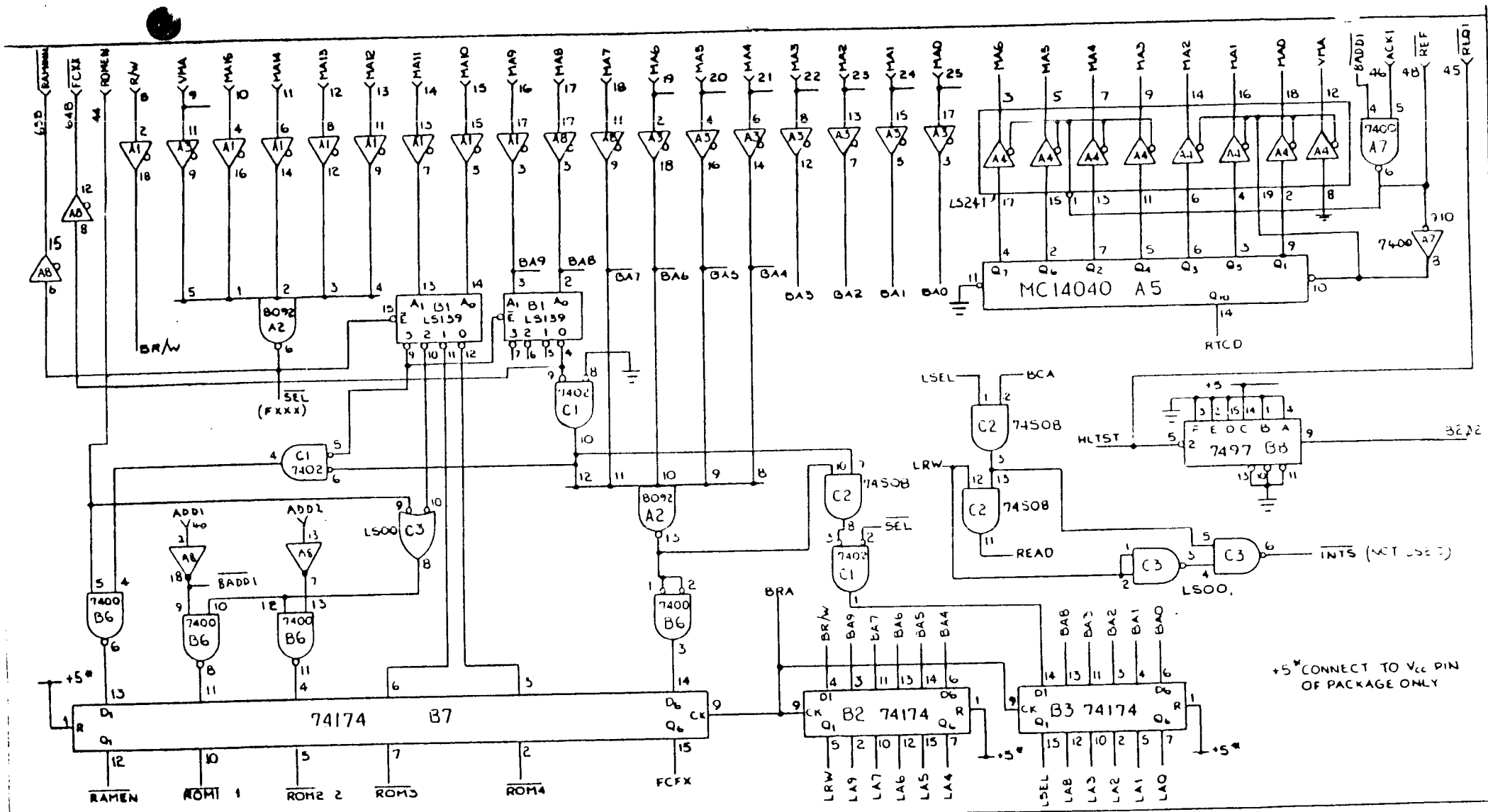
| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | CENTRAL PROCESSOR MODULE (SHEET 3 OF 3) BUS DRIVERS INTERRUPT LEVEL MUX 0 A S A R 0 0 2 6 SHEET 3 of 3 | | | |

| SCALE | | PASSED | DATE |
|---|---|---|---|
| NIL | | | 26/8/75 |

FAIRLIGHT INSTRUMENTS P/L
15 BOUNDARY STREET,
RUSHCUTTERS BAY 2011

| | |
|---|---|
| DRAWN | A G F |
| TRACED | P K |

DRAWING NUMBER
0 0 2 6 - 0 3
REV. 4




NOTE 74LS241 A1, A3 AND A8 - PIN 1 = GND, PIN 19 = +5 } ENABLES
A8 - PIN 2,13 = GND (SPARE BUFFERS)
PIN 18,7 = N/C

CENTRAL PROCESSOR CONTROL MODULE

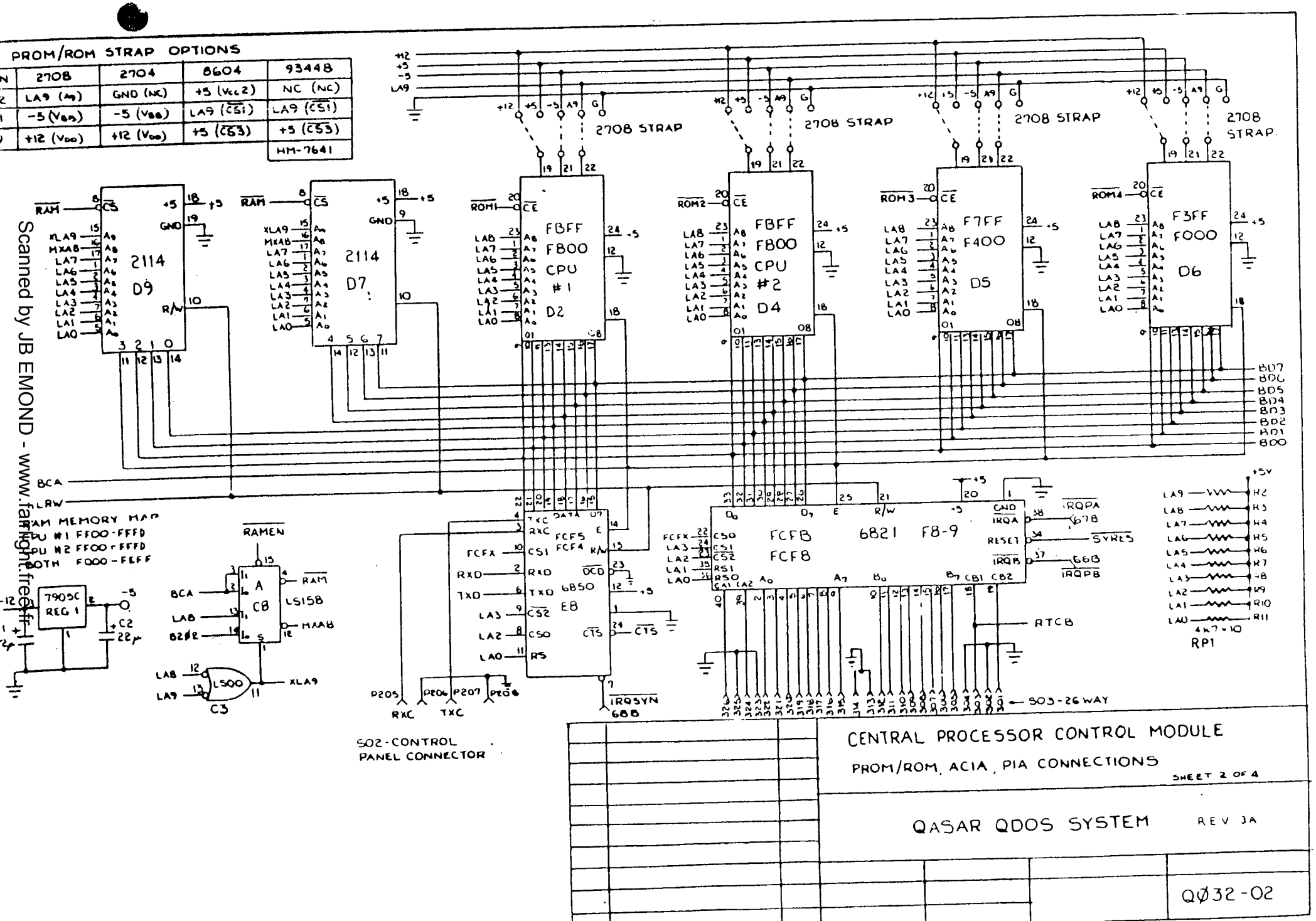
RAM/ROM/PROM DECODERS AND REFRESH LOGIC

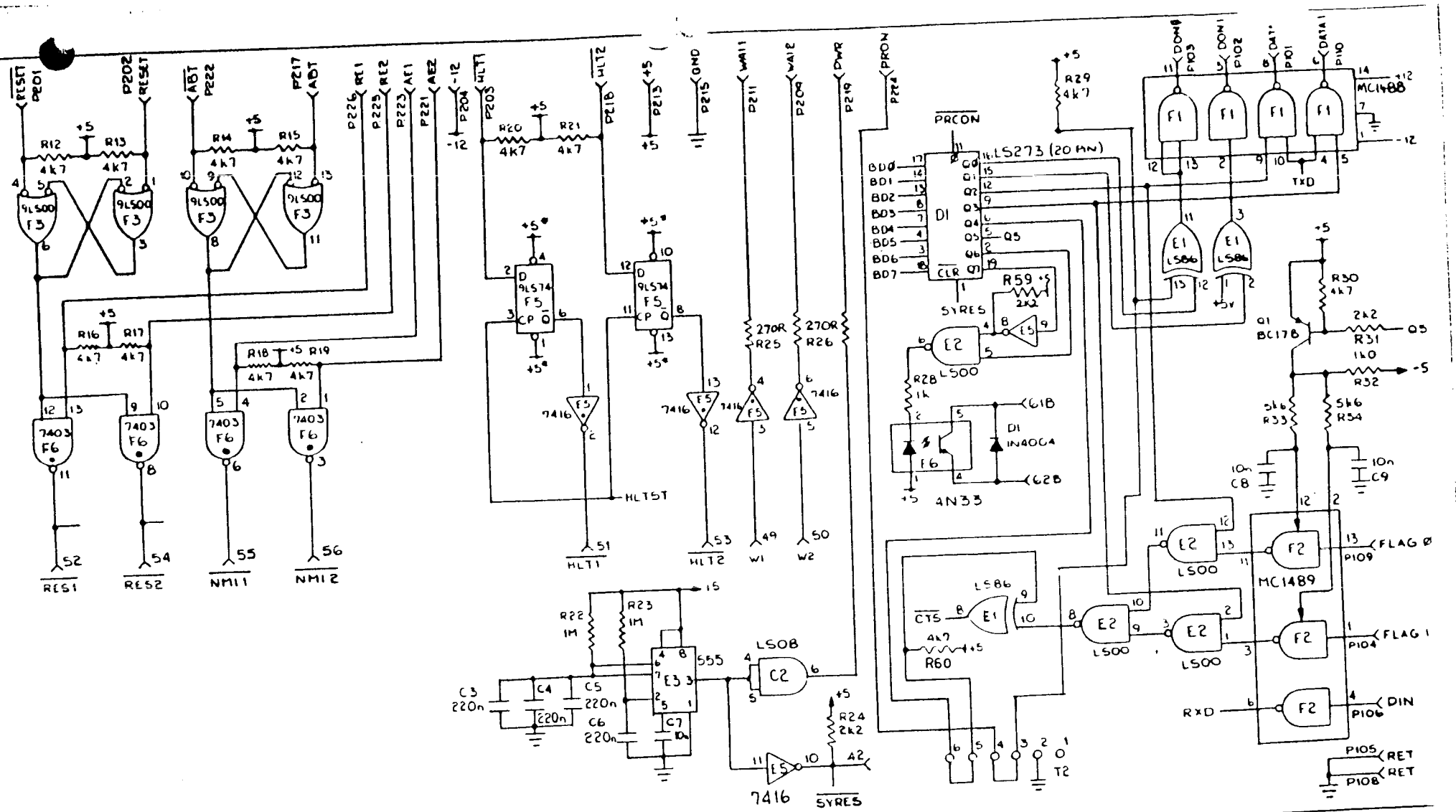
SHEET 1OF4

# QASAR QDOS SYSTEM

REV 3A

QØ32-Ø1





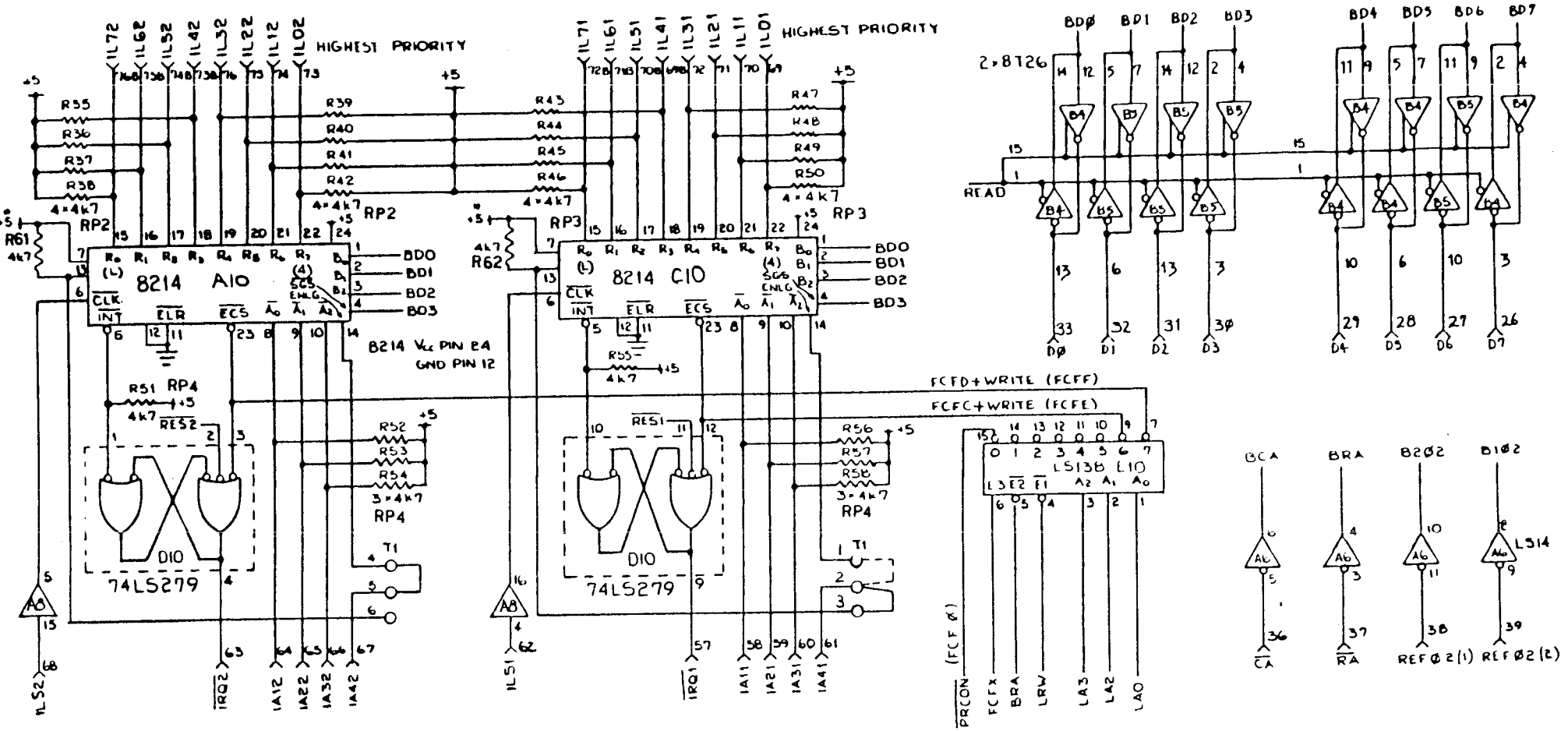

CENTRAL PROCESSOR CONTROL MODULE

TERMINAL INTERFACE AND MANUAL CONTROLS

SHEET 3 OF 4

QASAR QDOS SYSTEM REV 3A

0032-03




LINKS SHOWN INSTALLED ARE FOR CMI INTERRUPTS

--- QAGAR

+5* CONNECT TO Vcc OF PACKAGE

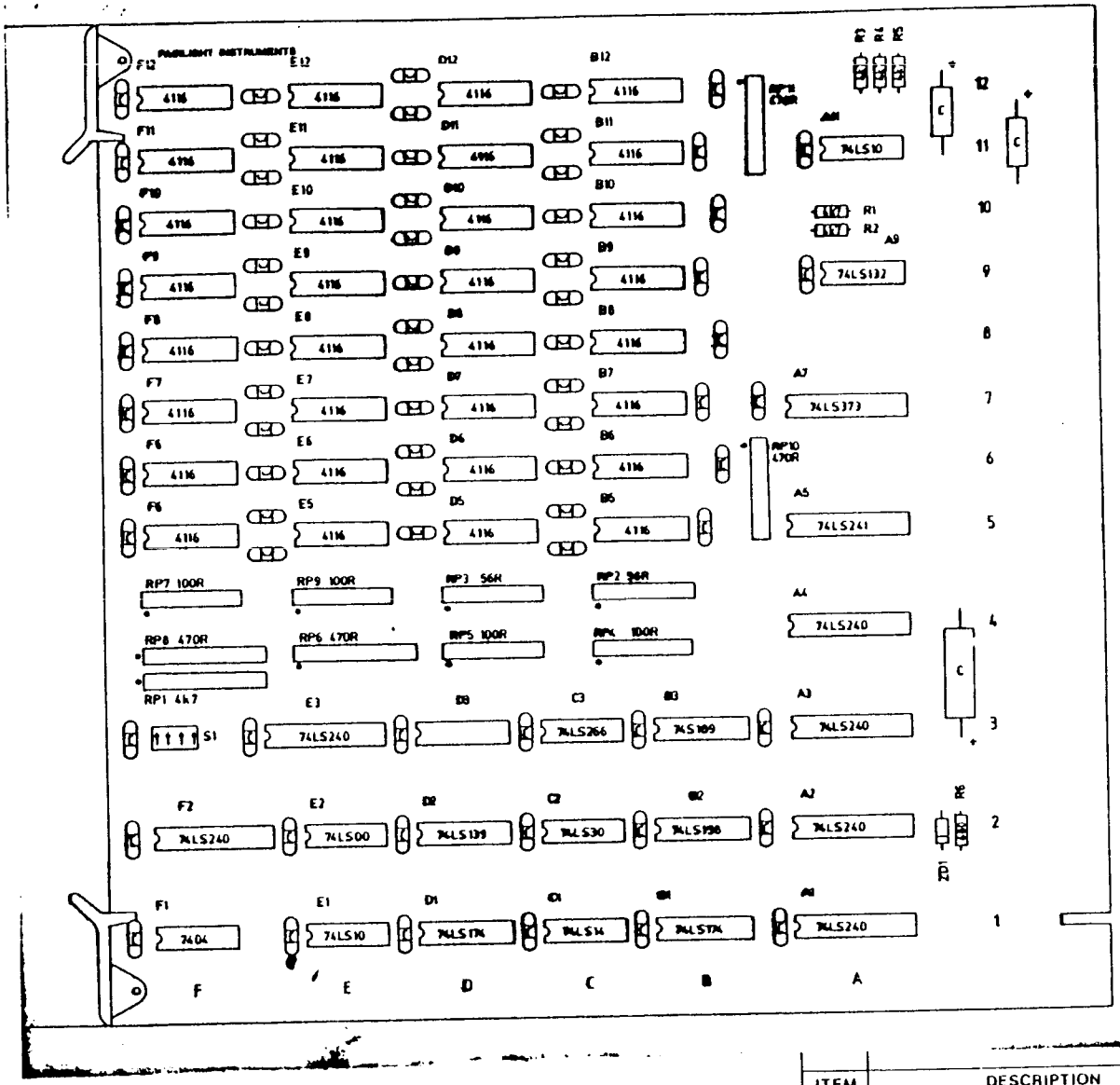
| | | |
|---|---|---|
| 2101 | LINKS FOR INTERRUPTS | C1 |

CENTRAL PROCESSOR CONTROL MODULE

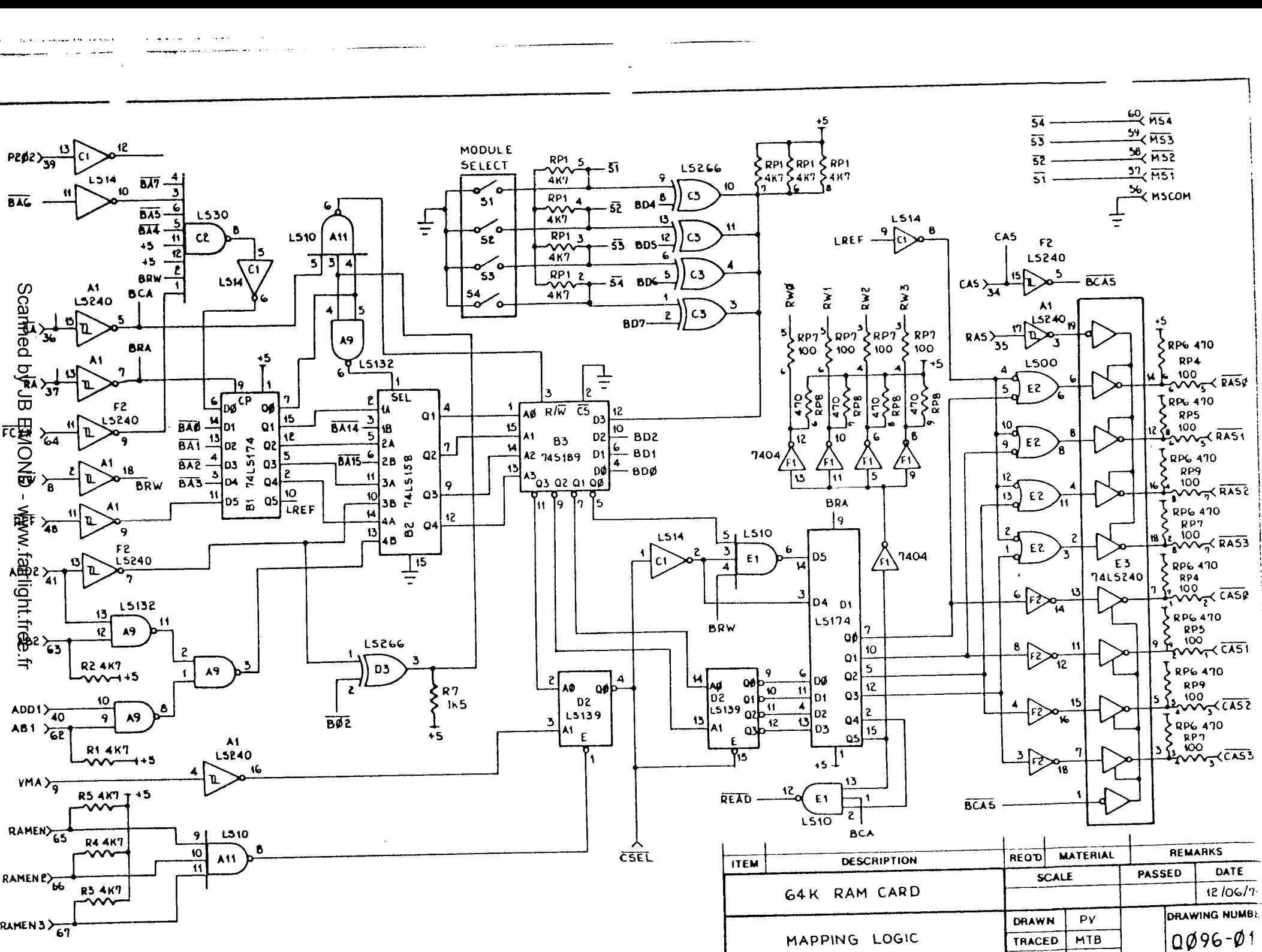
INTERRUPT PRIORITY LOGIC & DATA BUFFERS SHEET 4 OF

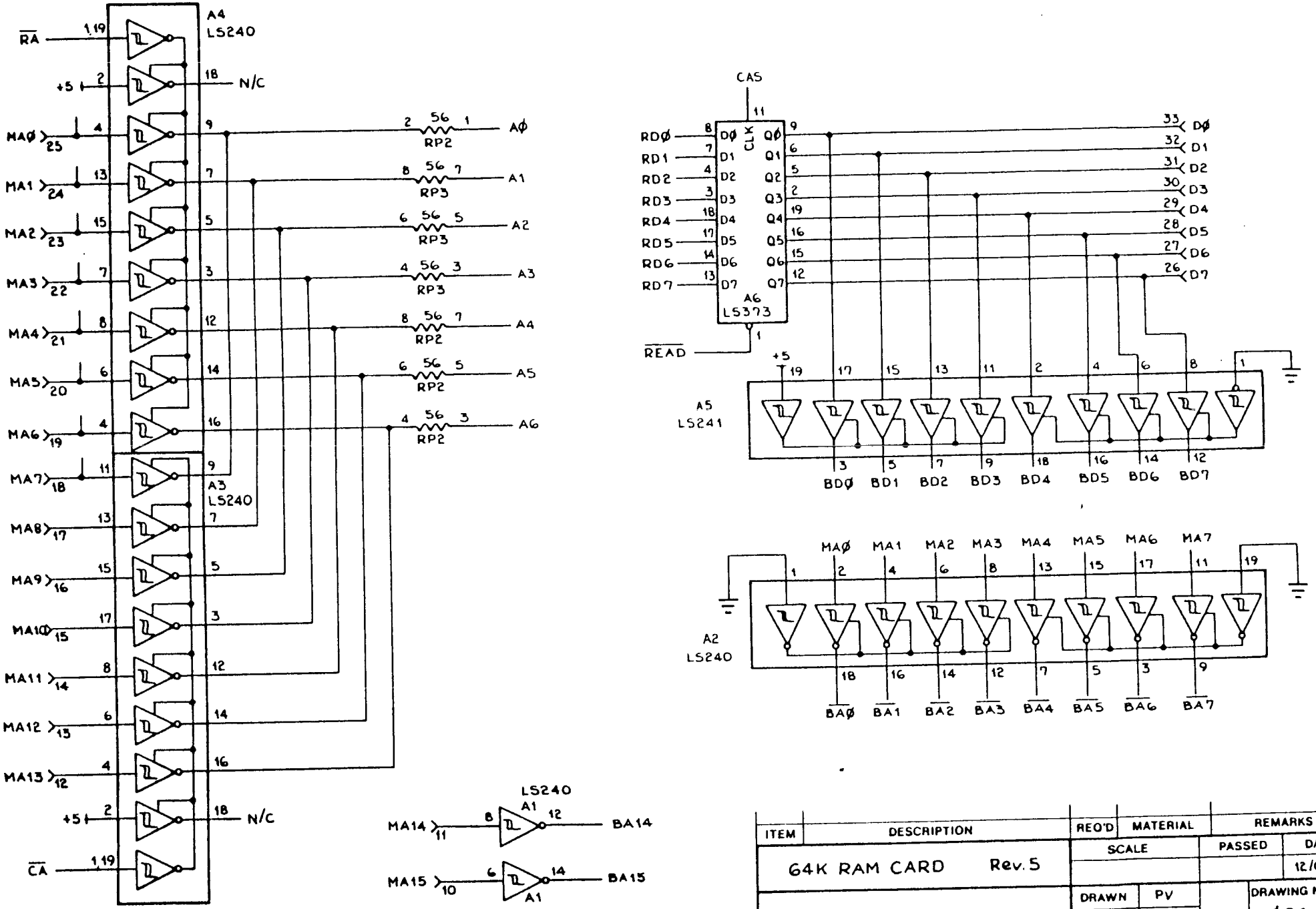
QASAR QDOS SYSTEM REV 3A

| DRAWN | CHECKED | SCALE | |
|---|---|---|---|
| | | | QØ32-04 |

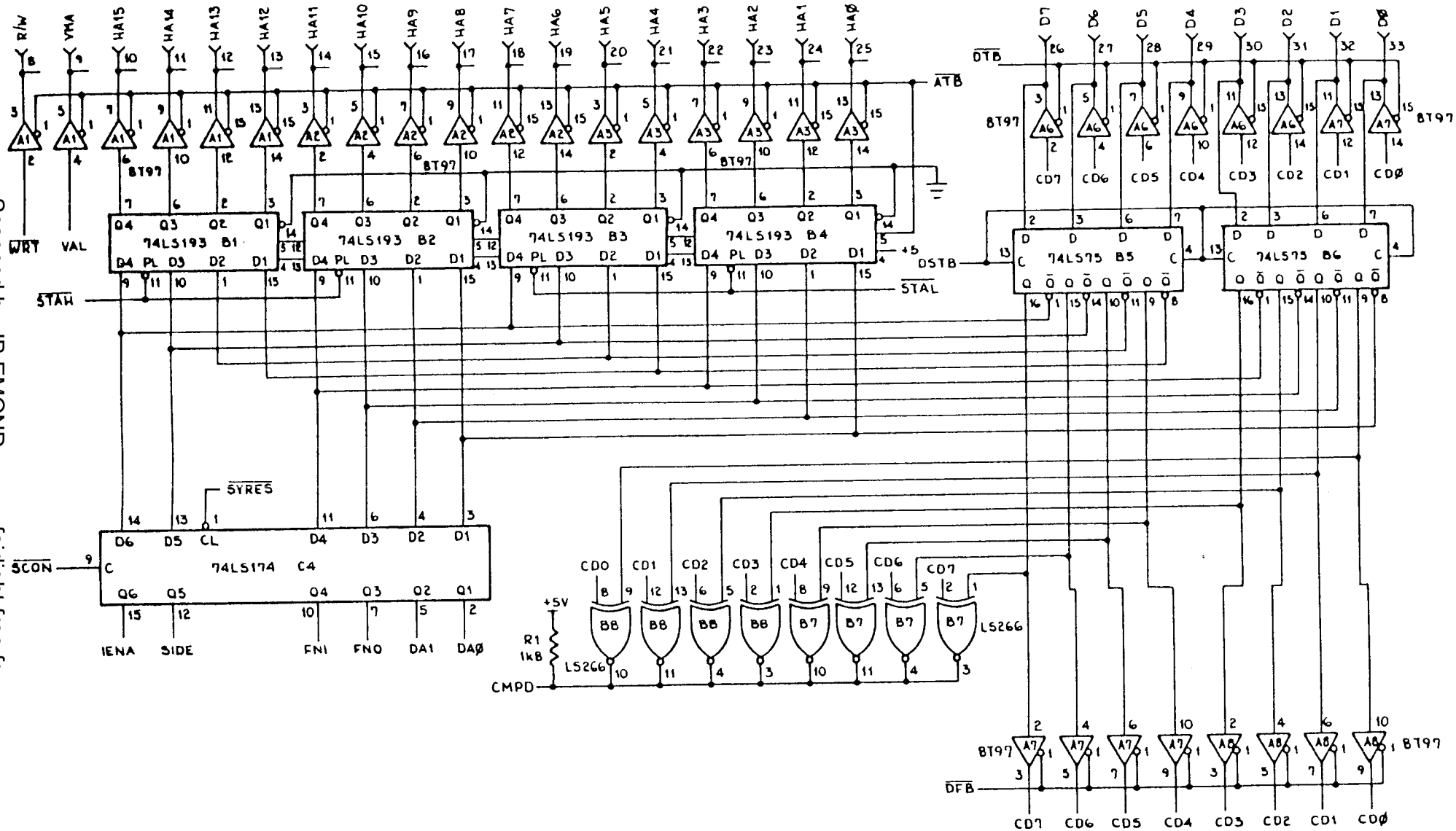



| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | | SCALE | | PASSED / DATE |
| OVERLAY for 64K RAM CARD Q096 Rev5 | | DRAWN / TRACED / CHECKED | | DRAWING NUM Q096-0 |

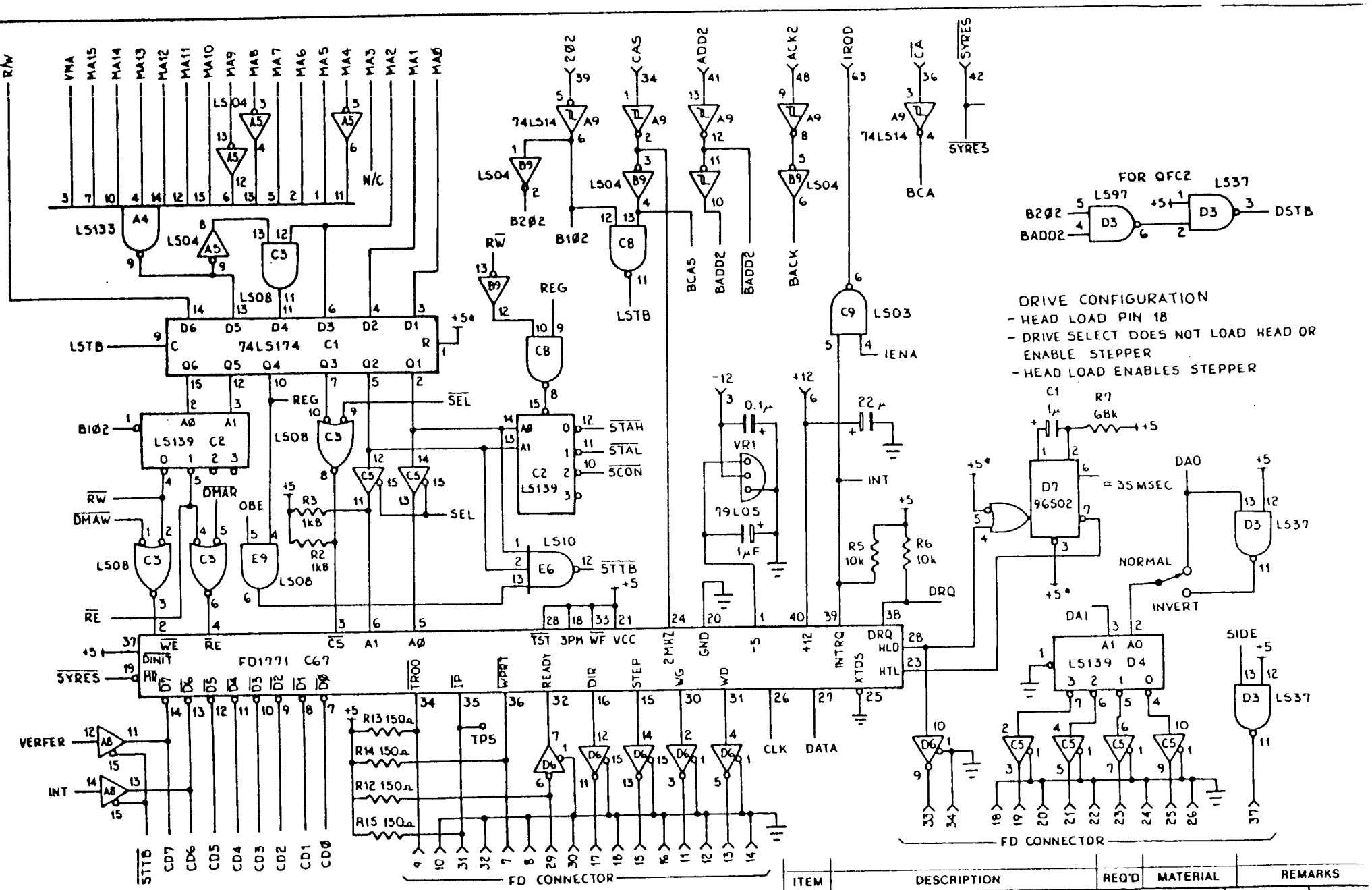





| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | 64K RAM CARD Rev.5 | SCALE | | PASSED / DATE 12/06/ |
| | BUS INTERFACE | DRAWN PV / TRACED MTB | | DRAWING NUM 0096-Ø |



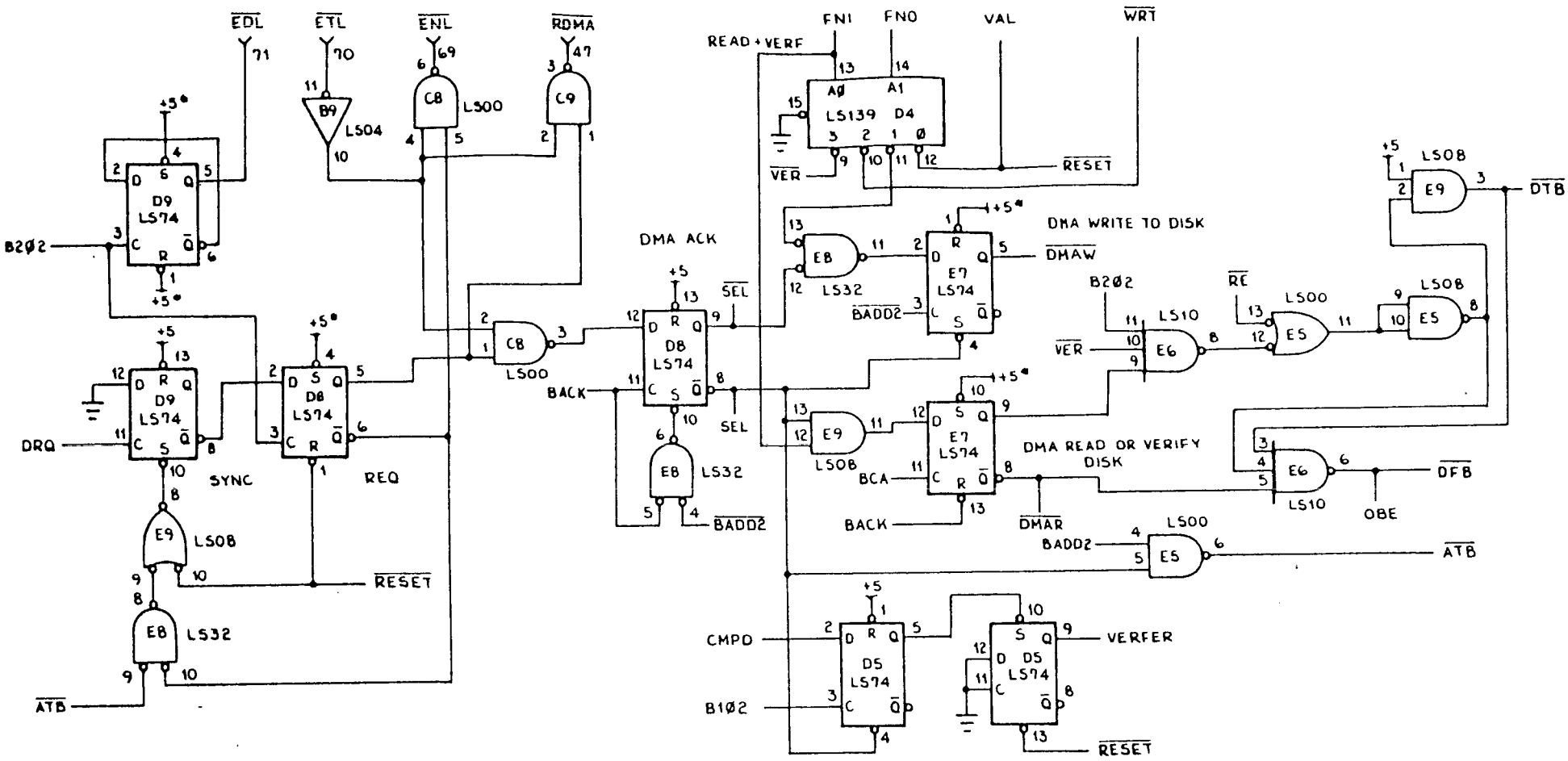

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FLOPPY DISK CONTROLLER/FORMATTER REV 3 | | SCALE | | PASSED / DATE 27/1/77 |
| DATA BUFFERS, DMA ADDRESS COUNTER, VERIFY COMPARATOR | | DRAWN A.G.F. | TRACED M.T.B. | DRAWING NUMBER DFC2-Ø1 |



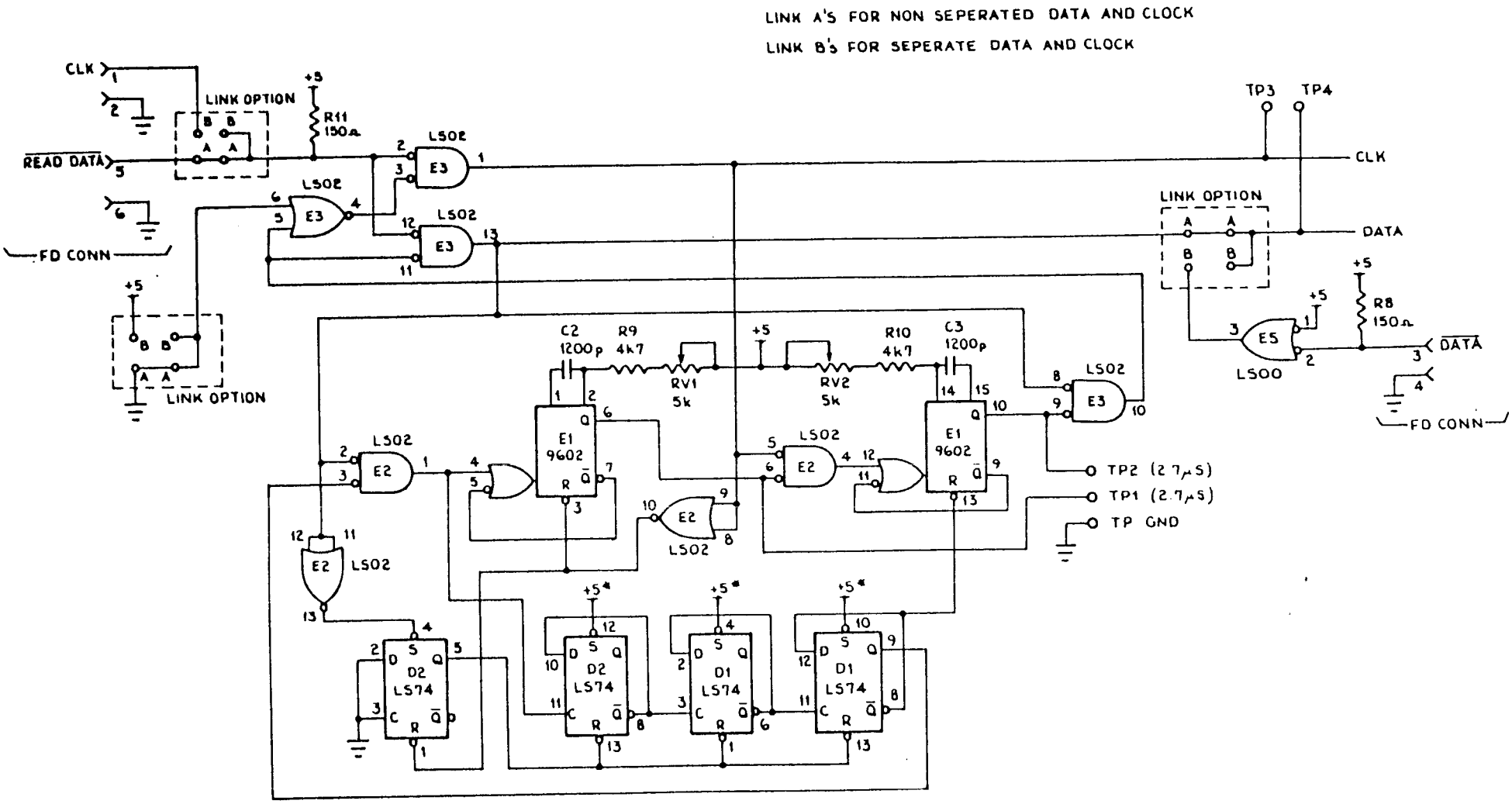

ADDRESSING

| | | | |
|---|---|---|---|
| FCE0 | FDC | FCE4 | DMA ADD HI |
| FCE1 | | FCE5 | DMA ADD LO |
| FCE2 | | FCE6 | DMA CONT. |

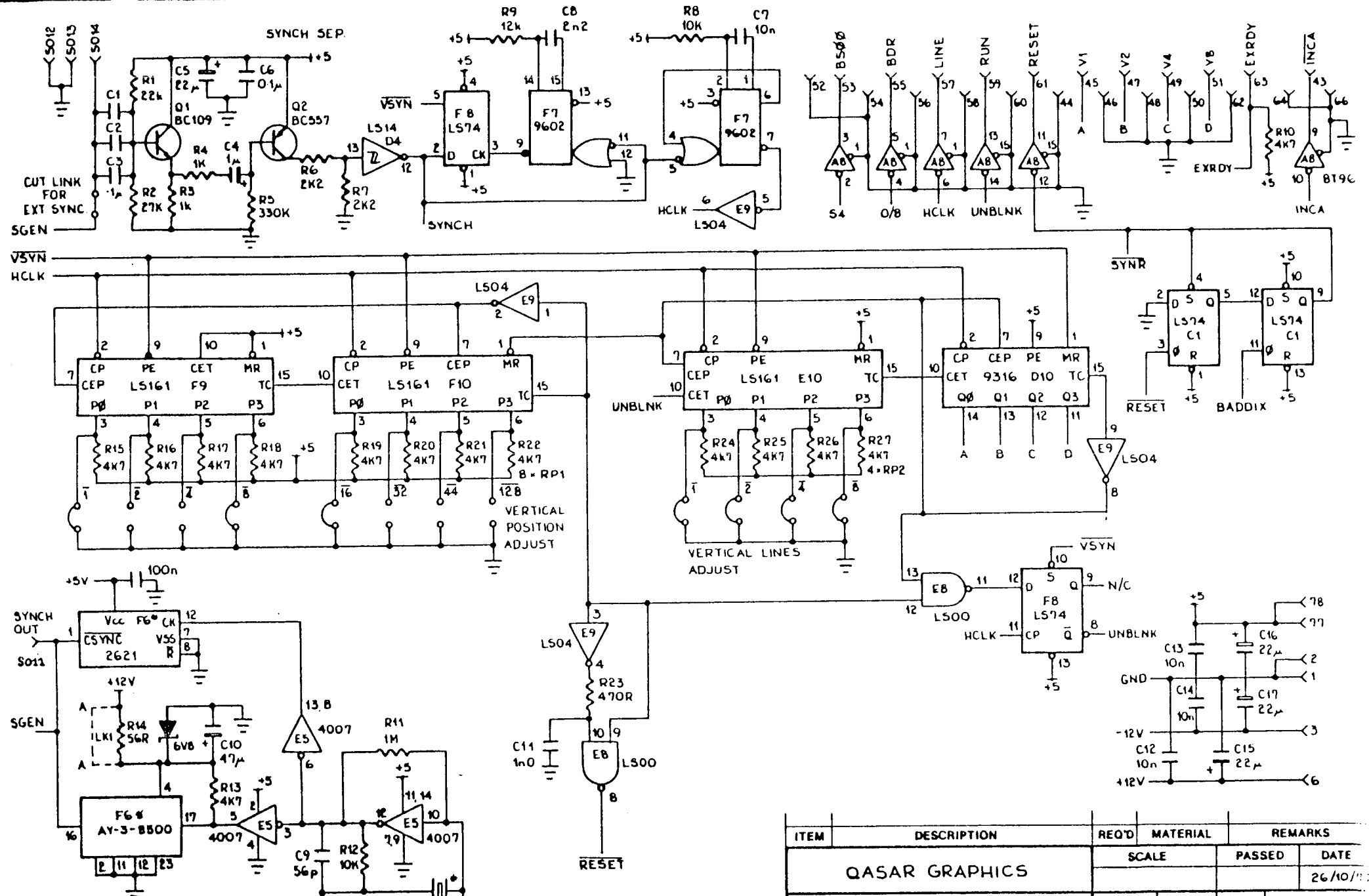
| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | FLOPPY DISK CONTROLLER/FORMATTER REV. 3 | SCALE | | PASSED / DATE 27/1/7 |
| | ADDRESS DECODING, CONTROLER | DRAWN AGF | | DRAWING NUM QFC2 1 |



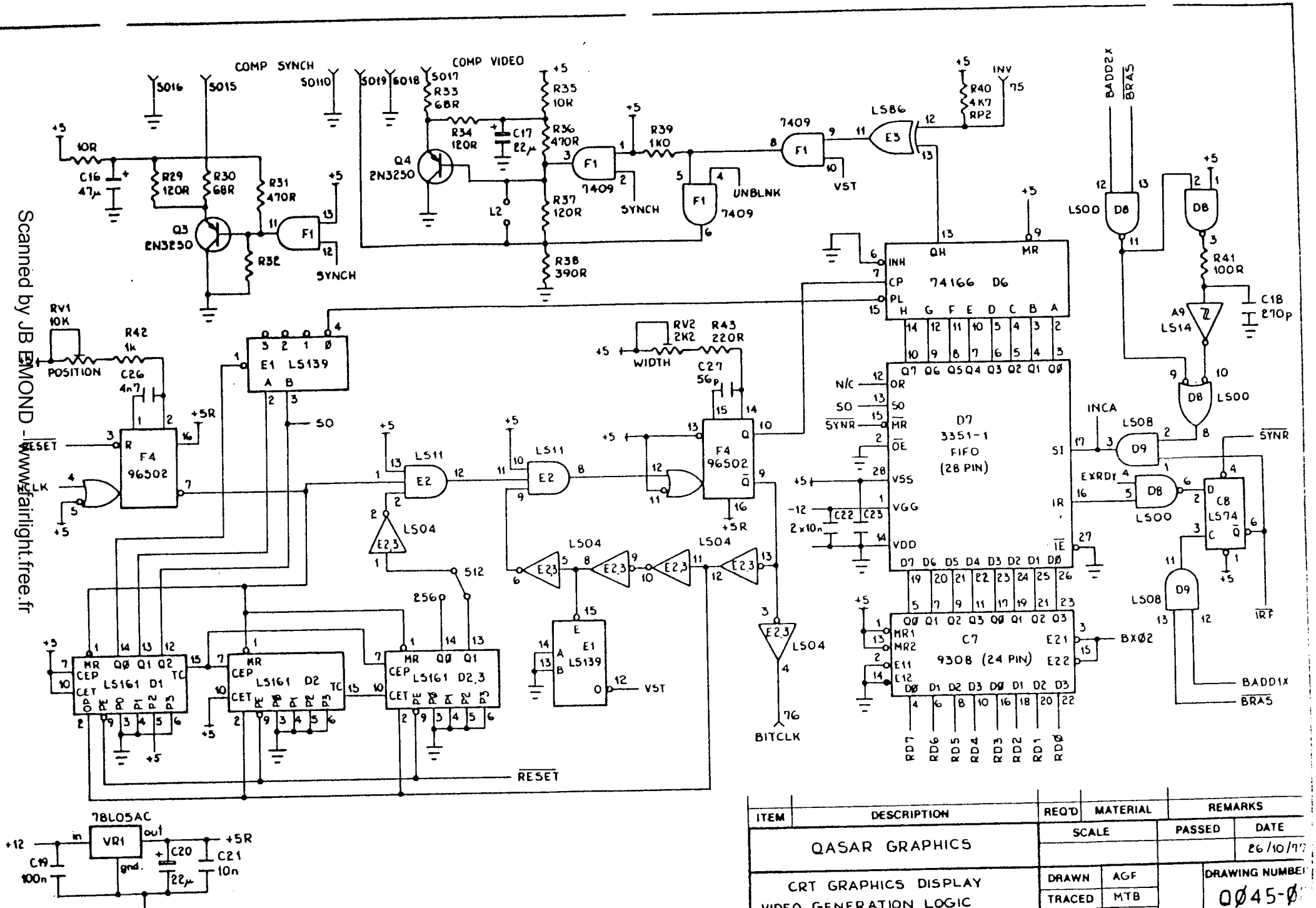

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FLOPPY DISK CONTROLLER FORMATTER REV. 3 | | SCALE | | PASSED / DATE 28/1/77 |
| | DMA LOGIC | DRAWN AGF | | DRAWING NUMBER |



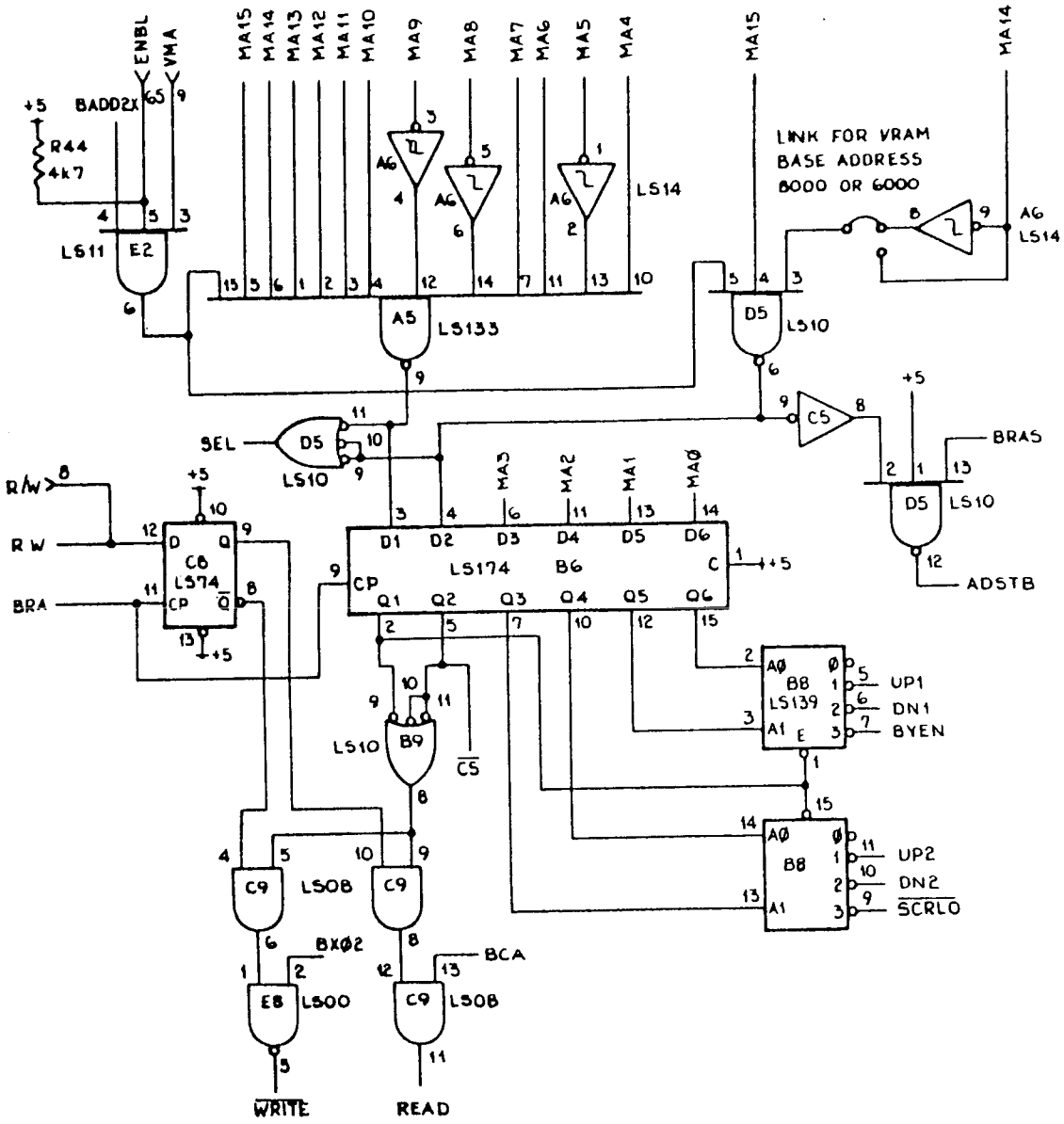

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FLOPPY DISK CONTROLLER FORMATTER REV. 3 | | SCALE | | PASSED / DATE 28/1/77 |
| DATA SEPERATOR | | DRAWN AGF<br>TRACED MTB | | DRAWING NUMBER QFC2-04 |

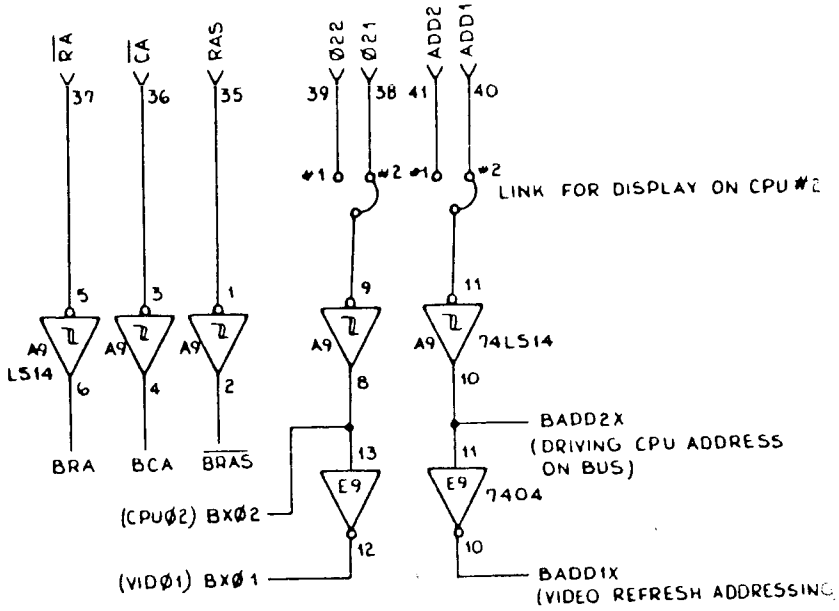


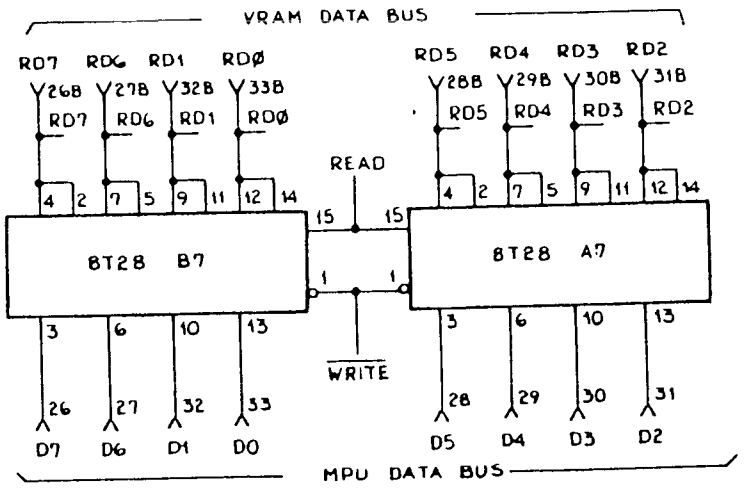

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | QASAR GRAPHICS | SCALE | | PASSED / DATE 26/10/ |
| | CRT GRAPHICS DISPLAY | DRAWN AGF | | DRAWING NUMB |
| | | TRACED MJB | | |



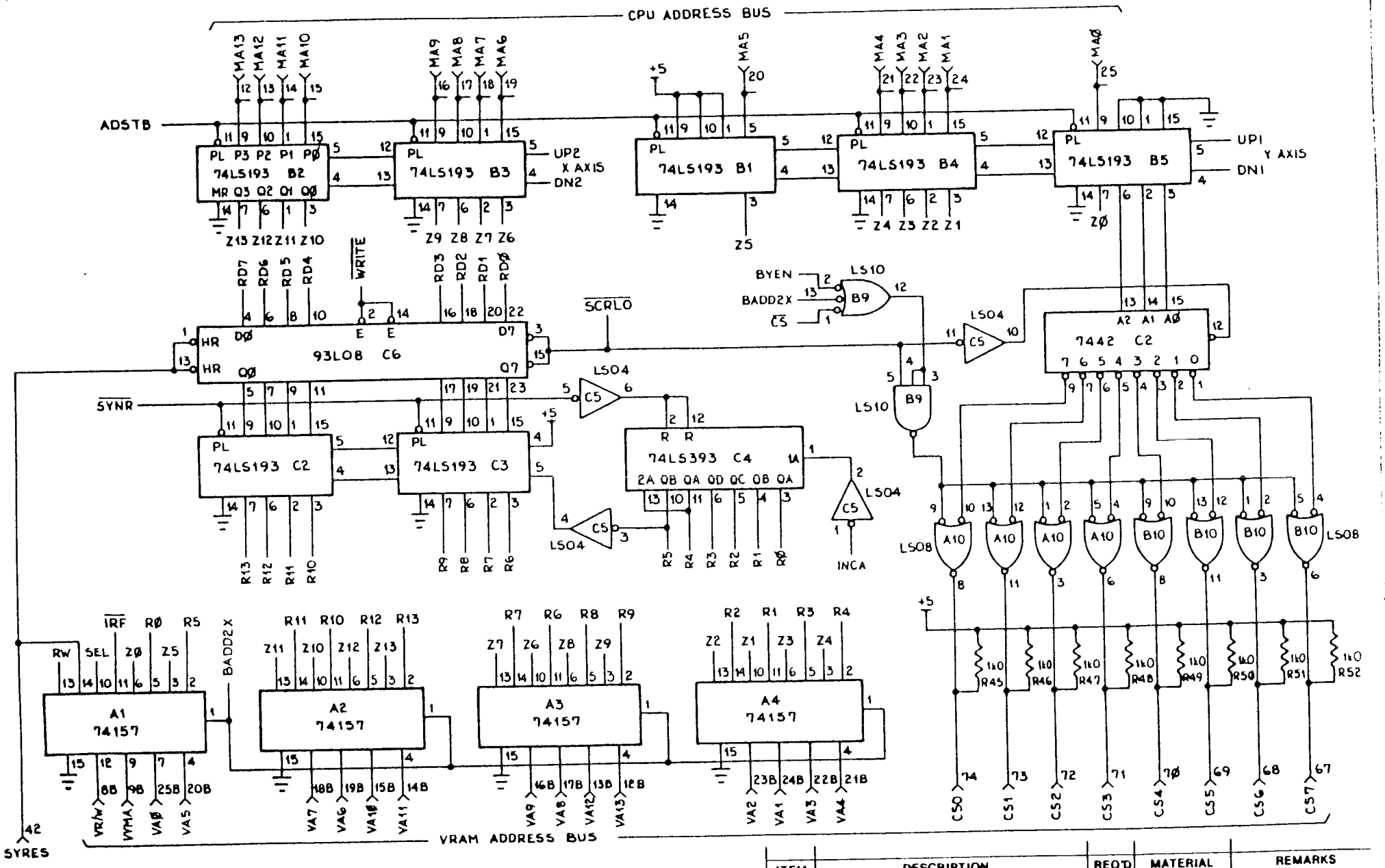

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | QASAR GRAPHICS | SCALE | | PASSED / DATE 26/10/77 |
| | CRT GRAPHICS DISPLAY VIDEO GENERATION LOGIC | DRAWN AGF / TRACED MTB | | DRAWING NUMBER 0045-Ø |



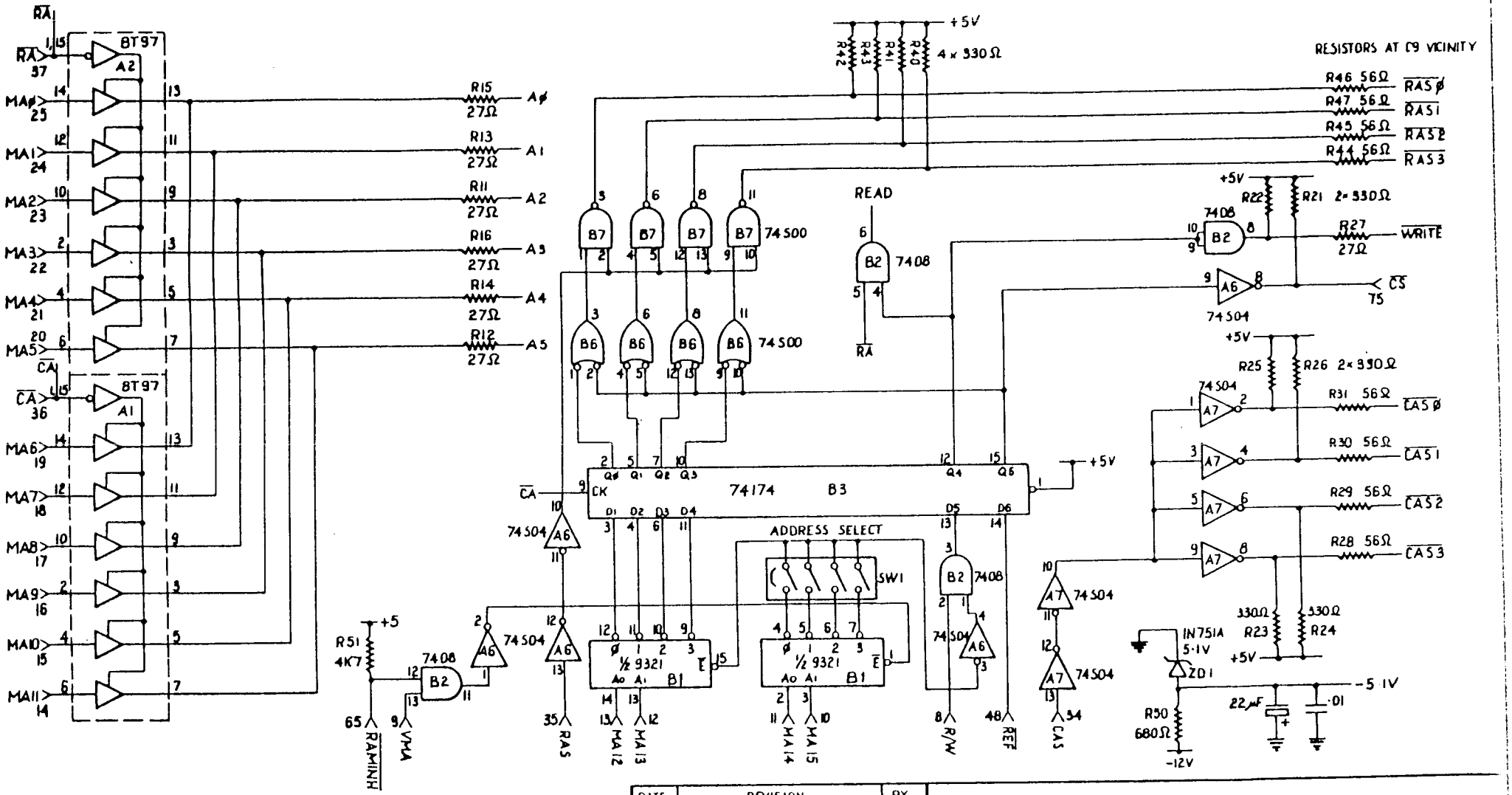




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | QASAR GRAPHICS | SCALE | | PASSED / DATE 29/10/ |
| | CRT GRAPHICS DISPLAY SELECT LOGIC AND DATA CONTROL | DRAWN AGF<br>TRACED MTB | | DRAWING NUM. 0045-0 |




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | QASAR GRAPHICS | SCALE | | PASSED / DATE 1/11/77 |
| | CRT GRAPHICS GENERATOR VRAM ADDRESSING LOGIC | DRAWN AGF | | DRAWING NUMB 0045-0 |
| | | TRACED MTB | | |



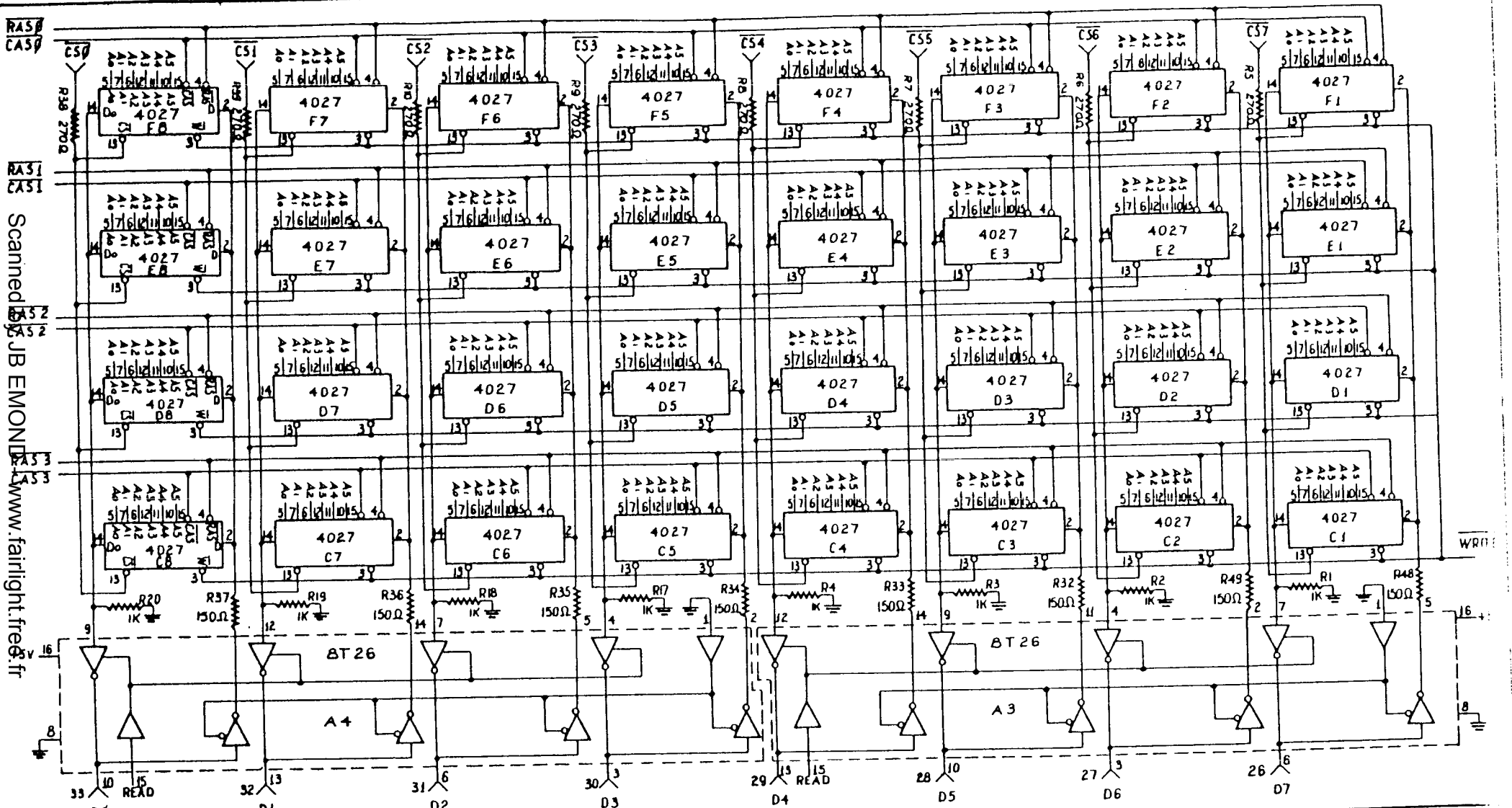

| DATE | REVISION | BY |
|---|---|---|
| 15·8·76 | 74265 ADDED | A.G.F. |
| 23·2·78 | RAMINH ADDED | D.K. |

# 16k BYTE MEMORY MODULE

SHEET 1 of 2

## BUSS INTERFACE AND ADDRESS DECODING

| DRAWN | CHECKED | SCALE | DRAWING N° |
|---|---|---|---|



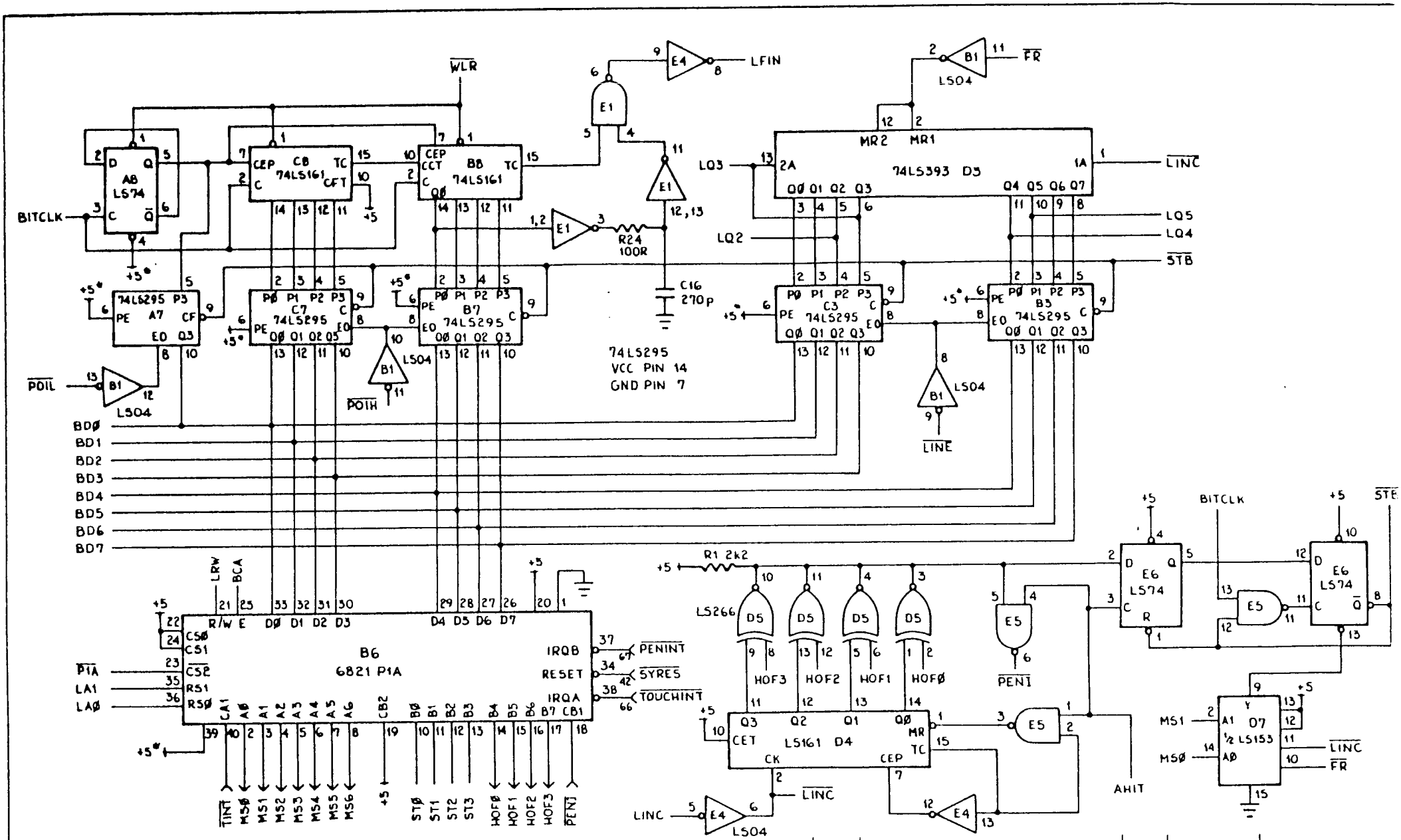

| DATE | REVISION | BY |
|---|---|---|
| 19·11·75 | $\overline{CS0}$ - $\overline{CS7}$ ADDED | A.G.F. |
| 15·8·75 | 1K, 150Ω, 270Ω RESISTORS ADDED | A.B.F. |
| 7·9·77 | CHANGED TO P.C. VERSION | D.K. |

# 16k BYTE MEMORY MODULE

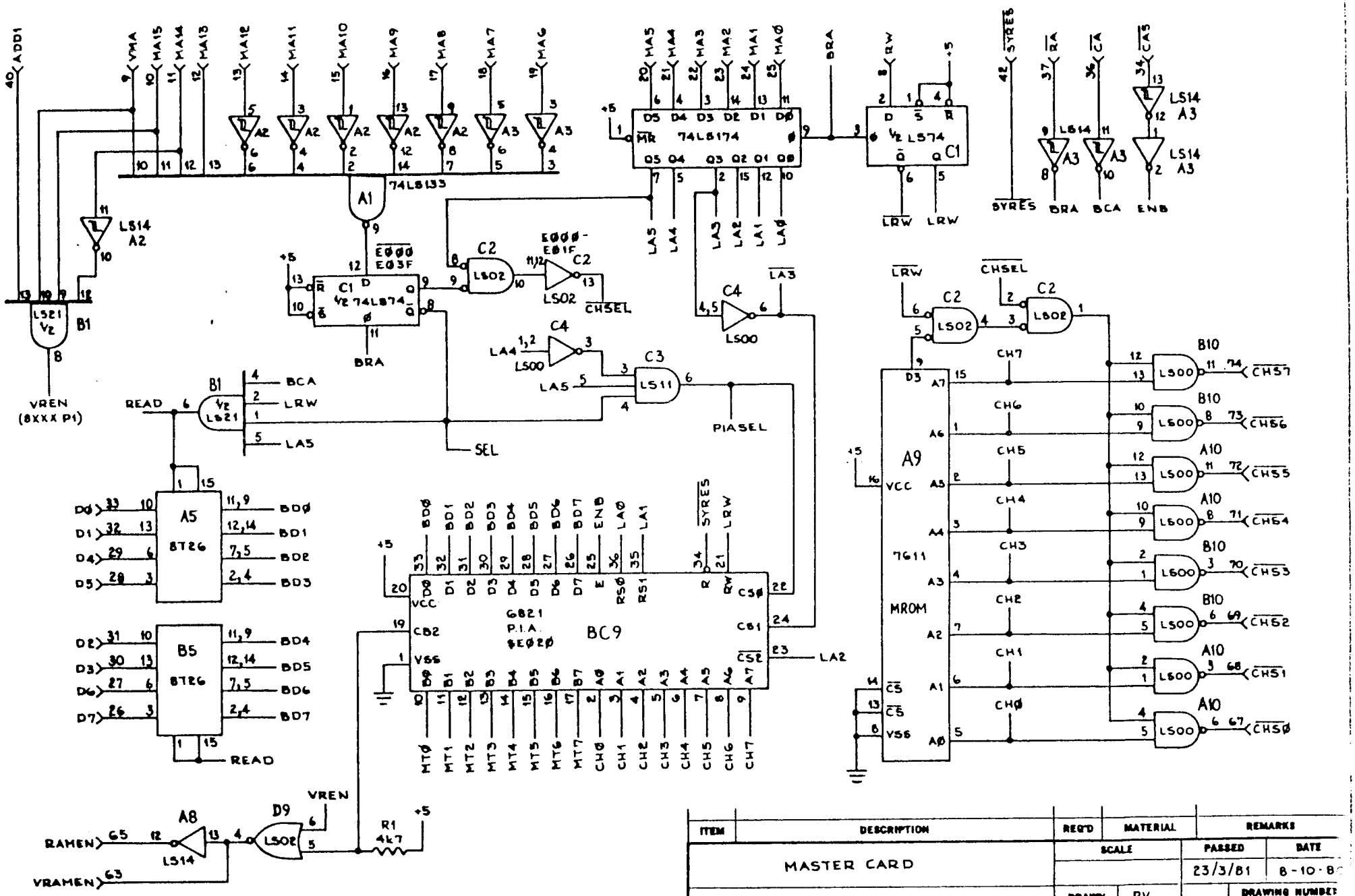
SHEET 2 of 2

## RAM ARRAY AND DATA BUFFERS

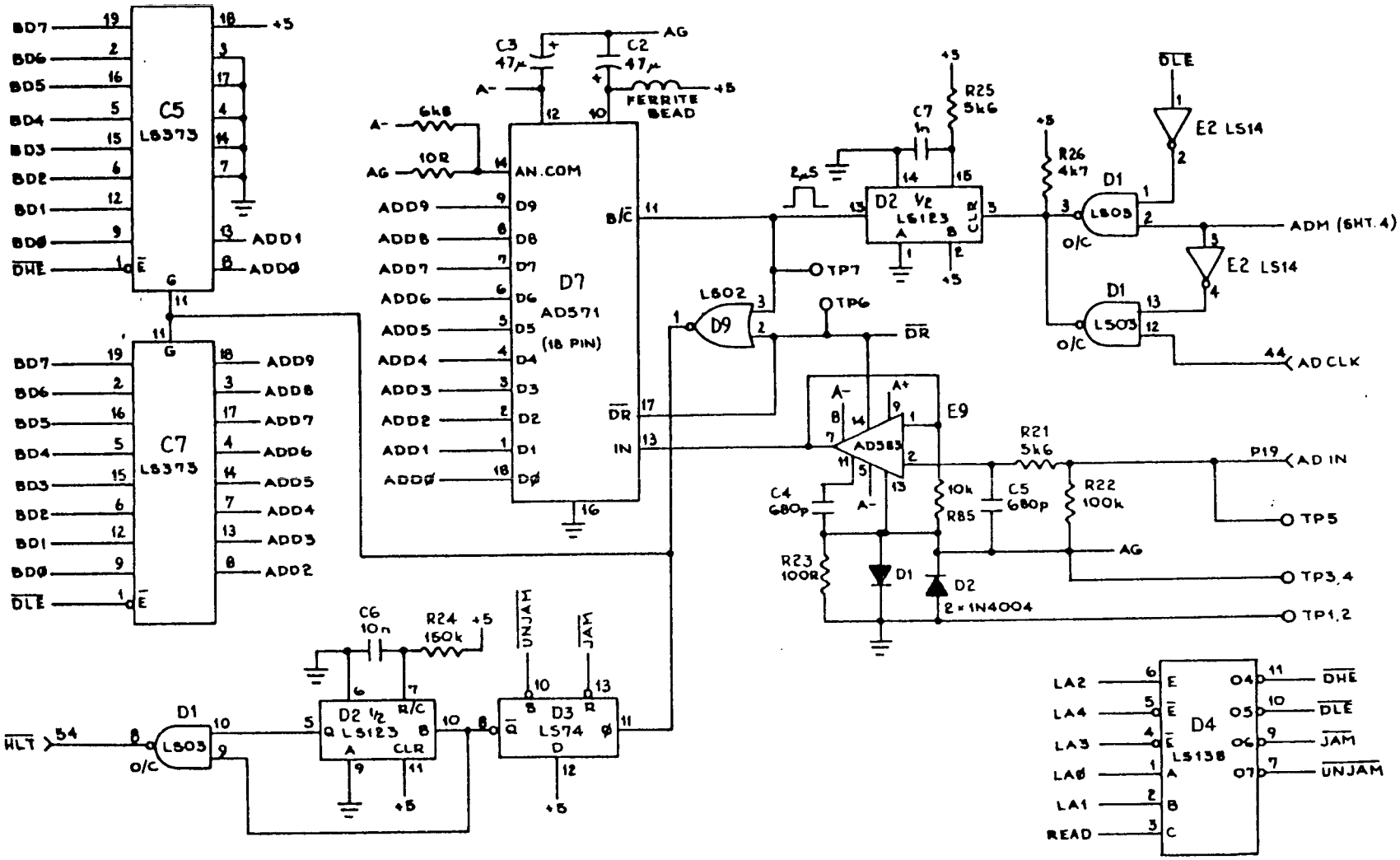
| DRAWN | CHECKED | SCALE | DRAWING N° |
|---|---|---|---|
| A.G.F. | R.V. | | C.025 - 02 |



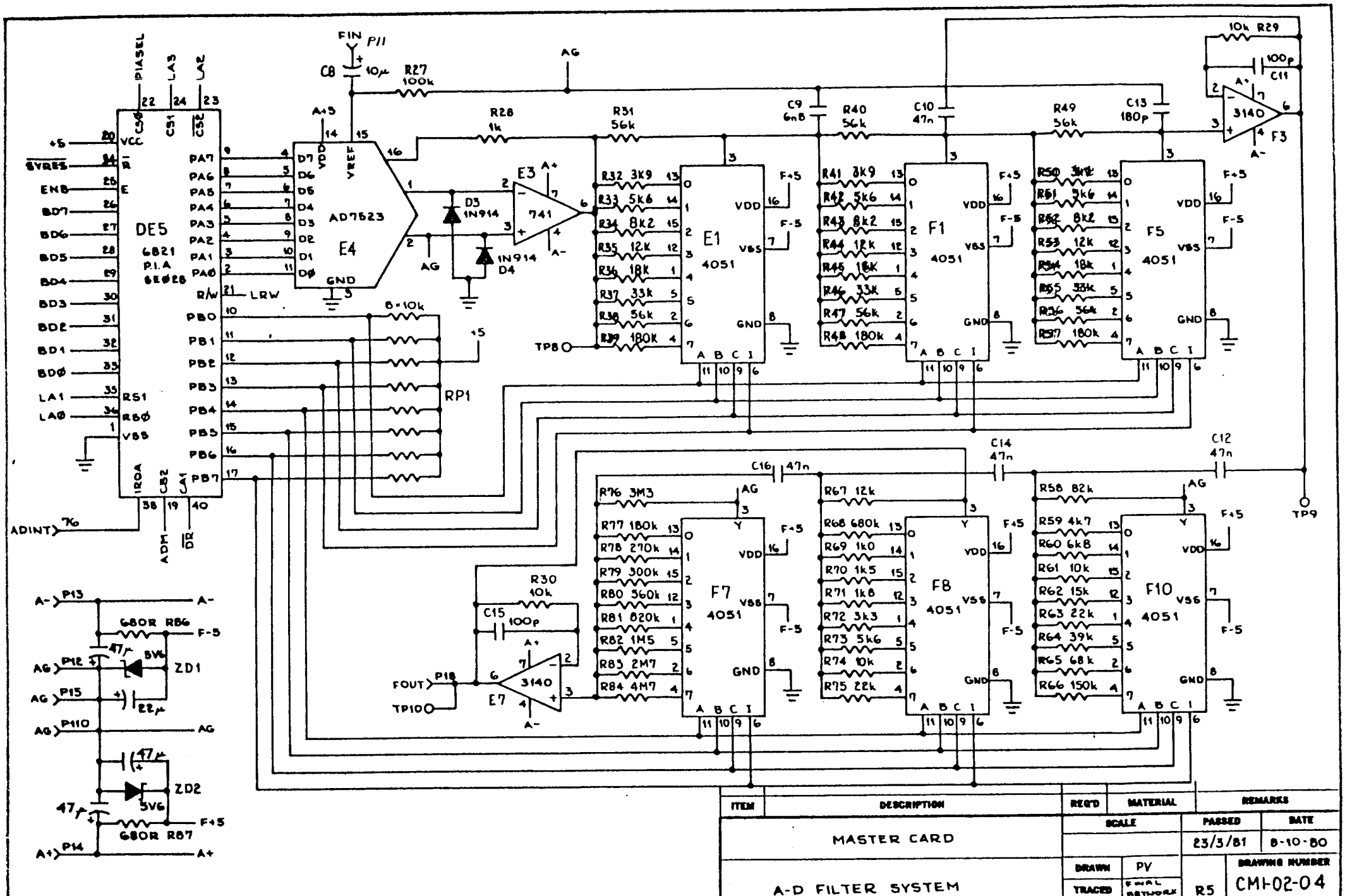

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | LIGHT PEN INTERFACE REV 4 | SCALE | | PASSED / DATE |
| | | | | 30/3/77 |
| | CO-ORDINATE COUNTERS, | DRAWN | AGF | DRAWING NUMB |




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | MASTER CARD | SCALE | | PASSED 23/3/81 DATE 8-10-8 |
| | ADDRESS DECODING; CHANNEL SELECTION RAM SWITCHING; | DRAWN PV | | DRAWING NUMBER R5 CM1-Ø2-Ø1 |



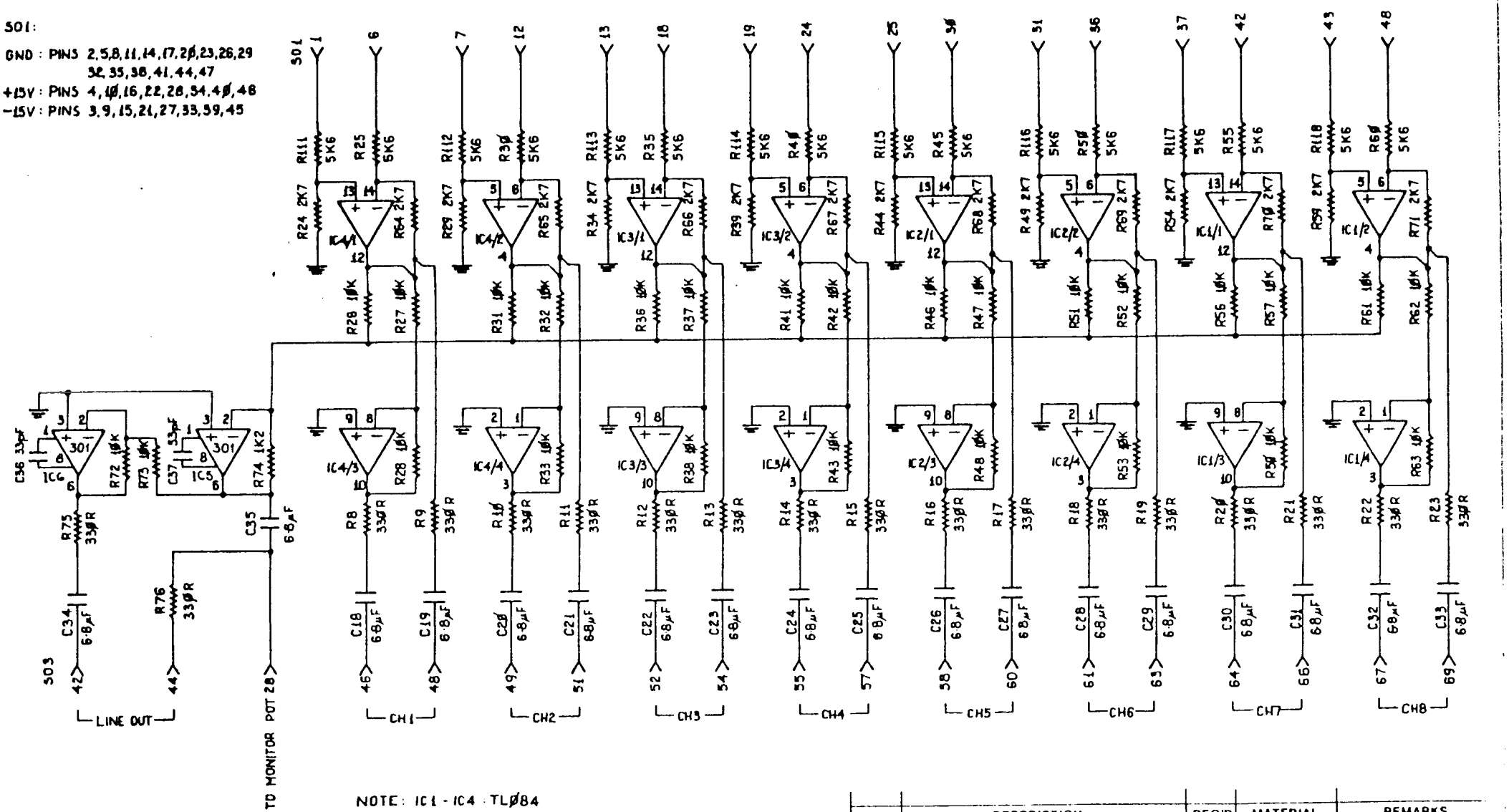

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | MASTER CARD | SCALE | | PASSED 23/3/81 DATE 7-10-80 |
| | AD CONVERTER | DRAWN PV | ENGL | R5 DRAWING NUMBER CM1-02-03 |




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | MASTER CARD | SCALE | PASSED 23/3/81 | DATE 8-10-80 |
| | A-D FILTER SYSTEM | DRAWN PV | R5 | DRAWING NUMBER CMI-02-04 |
| | | TRACED | | |

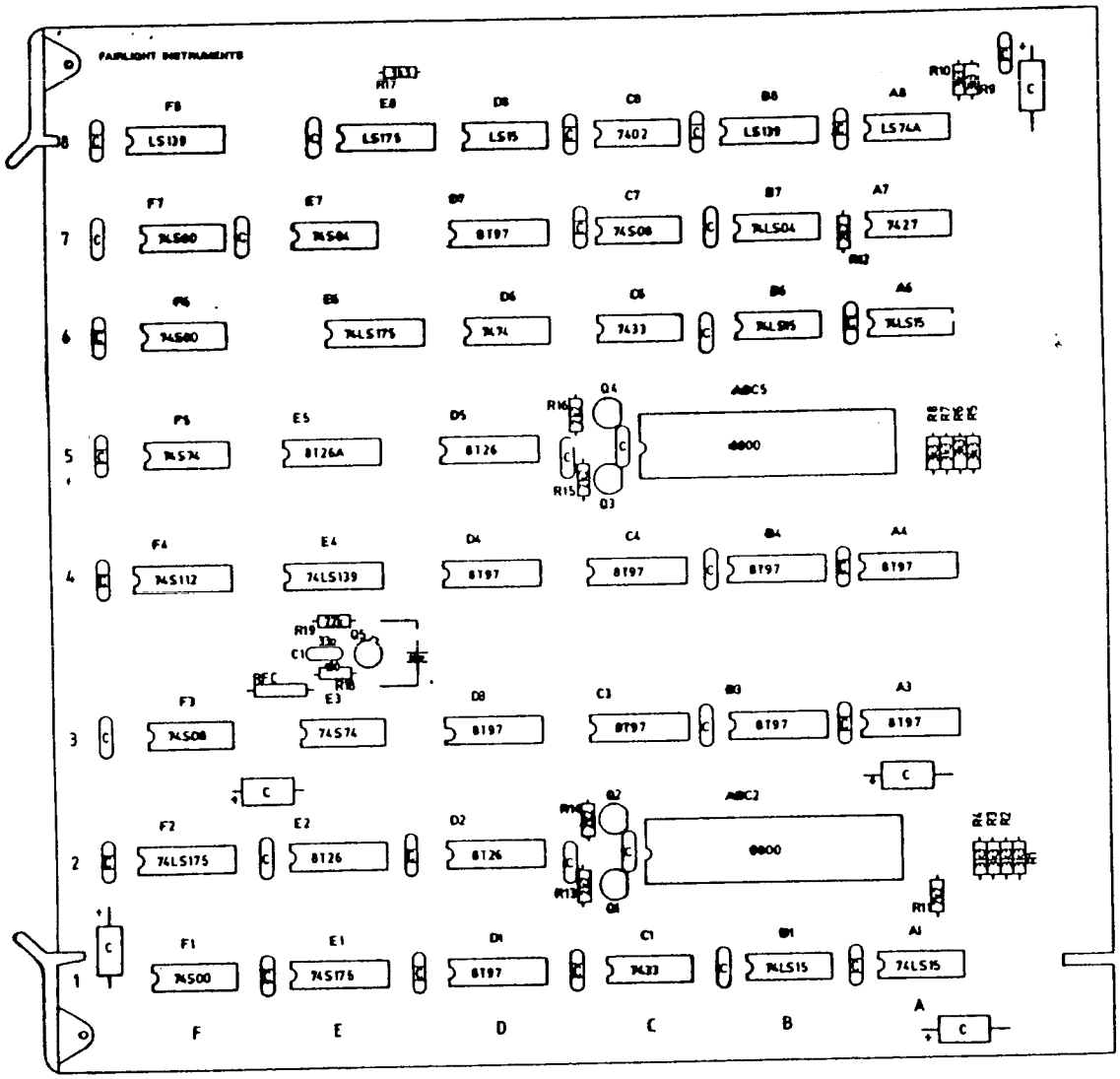
12.9 CMI01 SCHEMATIC

** NOT FOR PUBLICATION **

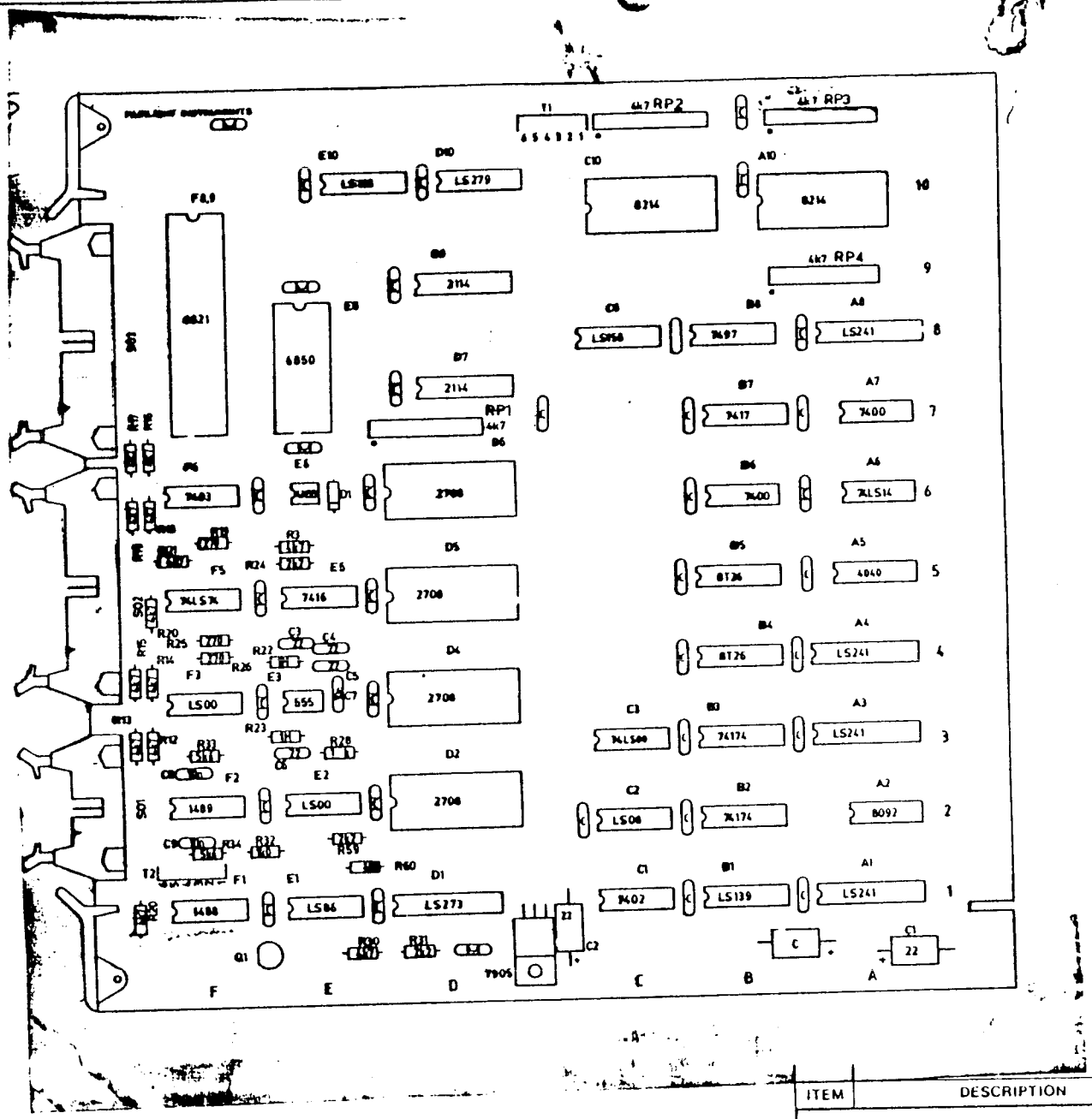



NOTE: IC1 - IC4 - TL084

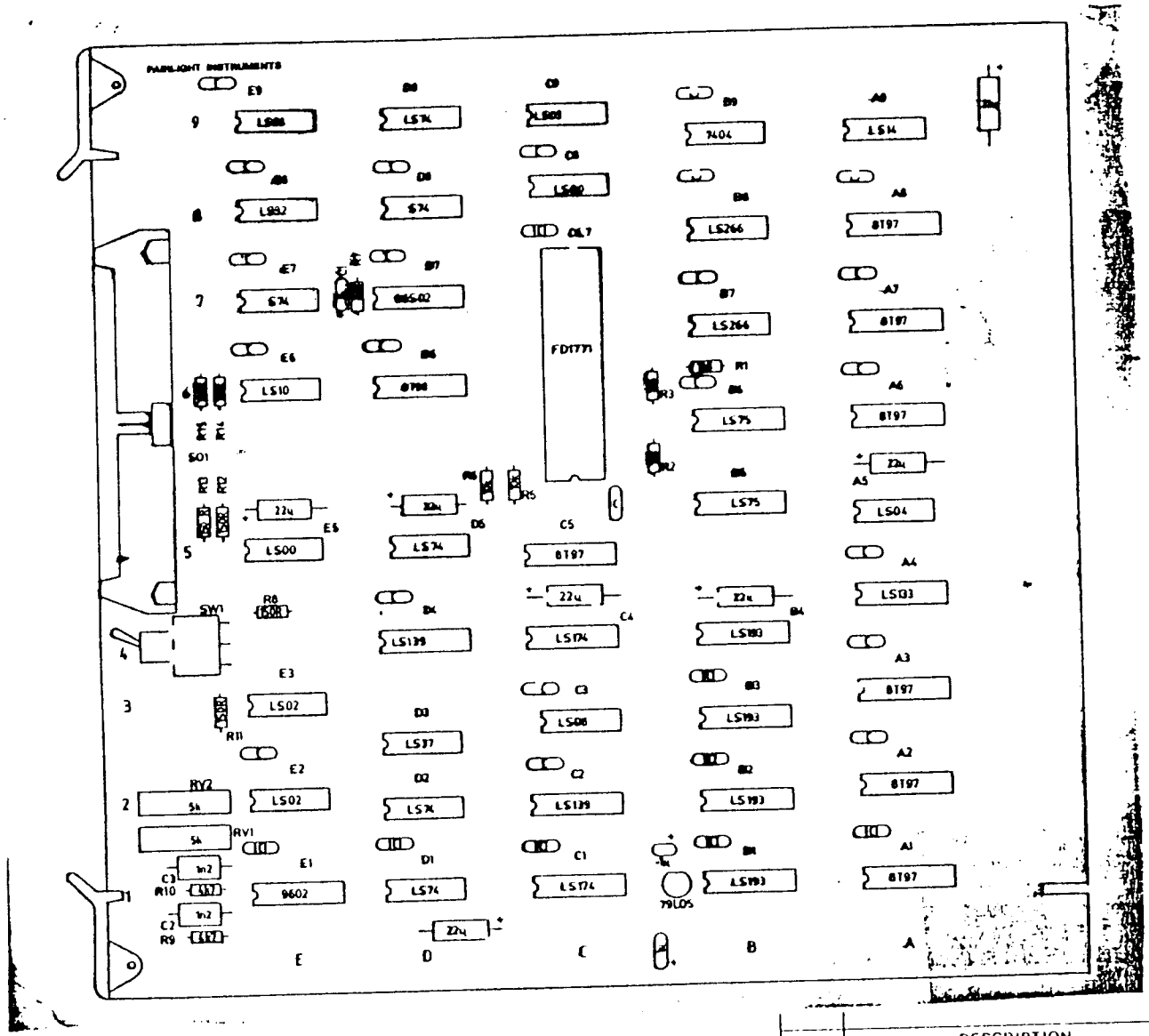
| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>15 BONDARY ST RUSHCUTTERS BAY 2011<br>(02) 335222 | | SCALE | | PASSED 1/7/1982 DATE 22/07/1979 |
| CMI AUDIO MODULE REV 4A1 | | DRAWN P V | | DRAWING NUMBER |



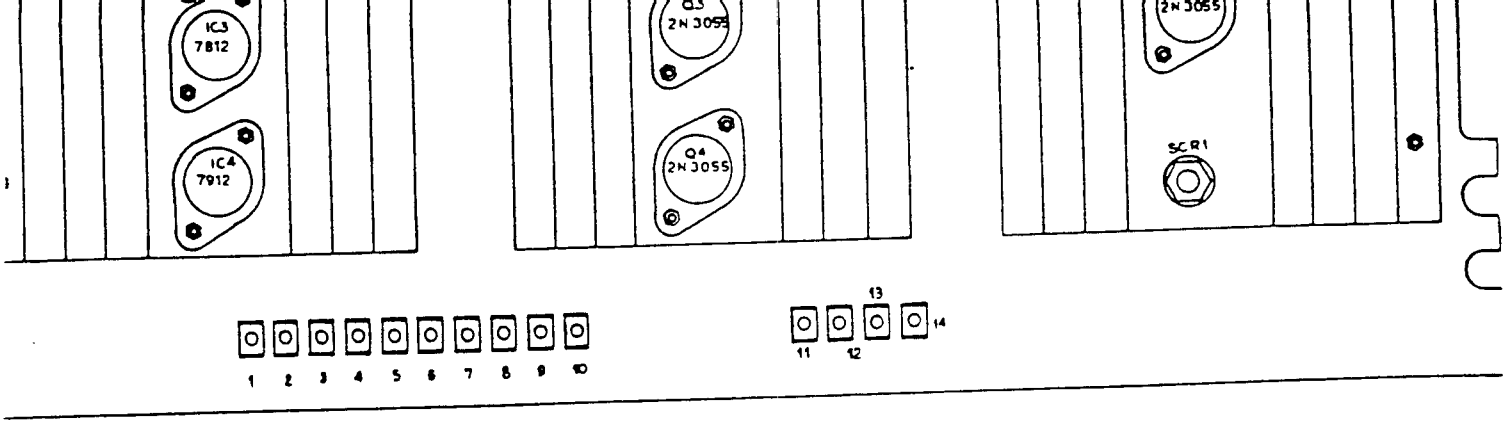

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | | SCALE | | PASSED / DATE |
| | | | | 7.7.82 |
| OVERLAY for CENTRAL PROCESSOR CARD Q026 R4 | | DRAWN | | DRAWING NUMBER Q026-04 |
| | | TRACED | | |
| | | CHECKED | | |



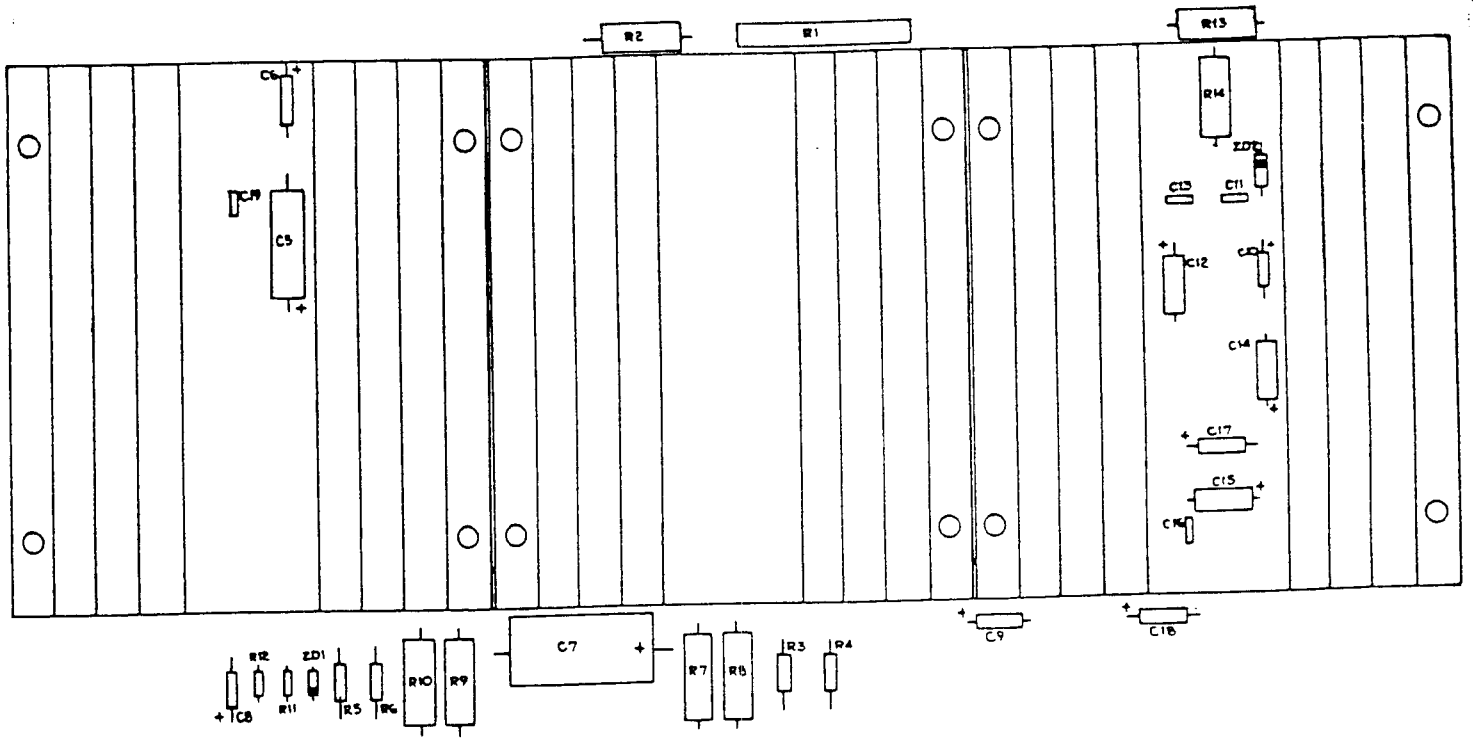

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | | SCALE | | PASSED / DATE |
| | | | | 7 7 8 |
| OVERLAY for CENTRAL PROCESSOR CONTROL CARD Q032 R3A | | DRAWN / TRACED / CHECKED | | DRAWING NUM: Q032-0 |




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | | SCALE | | PASSED / DATE |
| | | | | 7782 |
| OVERLAY For FLOPPY DISK CONTROLLER / FORMATTER QFC2 REV3 | | DRAWN | | DRAWING NUMBER |
| | | TRACED | | QFC2-05 |
| | | CHECKED | | |




FRONT SIDE OF P.C.B SHOWING
HEATSINKS AND BASEPLATE




COMPONENT SIDE OF P.C.B SHOWING HEATSINKS
(WITH BASEPLATE REMOVED)

14.0 ELECTRICAL PARTS LISTS

14.1 0026 DUAL 6800 PROCESSOR

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| A1 | 74LS15 | TRIPLE AND O.C. |
| A3,4 | 8T97 | HEX T.S. BUFFER |
| A6 | 74LS15 | TRIPLE AND O.C. |
| A7 | 7427 | TRIPLE NOR. |
| A8 | 74LS74 | DUAL F/FLOP |
| B1 | 74LS15 | TRIPLE AND O.C. |
| B2 | 6800 | CPU |
| B3,4 | 8T97 | HEX T.S.BUFFER |
| B5 | 6800 | CPU |
| B6 | 74LS15 | TRIPLE AND O.C. |
| B7 | 74LS04 | HEX INVERT |
| B8 | 74LS139 | DUAL DECODER |
| C1 | 7433 | QUAD NOR O.C. |
| C3,4 | 8T97 | HEX T.S. BUFFER |
| C6 | 7433 | QUAD NOR O.C. |
| C7 | 74S08 | QUAD AND. |
| C8 | 7402 | QUAD NOR. |

RESISTERS

| | |
|---|---|
| R1-R10 | 3K3 |
| R11-R16 | 2K2 |
| R17 | 3K3 |
| R18 | 180R |
| R19 | 22K |

TRANSISTORS

| | |
|---|---|
| Q1-Q4 | 2N3646 |
| Q5 | 2N2369 |

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| D1,3,4 | 8T97 | HEX T.S. BUFFER |
| D2,5 | 8T26 | QUAD BUS TXCVR. |
| D6 | 7474 | DUAL F/FLOP |
| D7 | 8T97 | HEX T.S. BUFFER |
| D8 | 74LS15 | TRIPLE AND O.C. |
| E1 | 74S175 | QUAD F/FLOP |
| E2 | 8T26 | QUAD BUS TXCVR |
| E3 | 74S74 | DUAL F/FLOP |
| E4 | 74LS139 | DUAL DECODER |
| E5 | 8T26 | QUAD BUS TXCVR |
| E6 | 74LS175 | QUAD F/FLOP |
| E7 | 74S04 | HEX INVERT. |
| E8 | 74LS175 | QUAD F/FLOP |
| F1 | 74S00 | QUAD NAND |
| F2 | 74LS175 | QUAD F/FLOP |
| F3 | 74S08 | QUAD AND |
| F4 | 74S112 | DUAL F/FLOP |
| F5 | 74S74 | DUAL F/FLOP |
| F6,7 | 74S00 | QUAD NAND |
| F8 | 74LS139 | DUAL DECODER |

CAPACITORS

| | | |
|---|---|---|
| C1 | 33PF | CERM. |
| 0.01UF | | MONO CERM. |
| 0.1UF | | MONO CERM. |
| 47UF | 25V | ELECT. |

CHOKE 1UH

CRYSTAL 40.21MHZ

## 14.2 6032 PROCESSOR CONTROL CARD

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| A1 | 74LS241 | OCTAL BUFFER |
| A2 | 8092/7092 | DUAL DECOD. |
| A3,4 | 74LS241 | OCTAL BUFFER |
| A5 | 4040 | BINARY COUNTER |
| A6 | 74LS14 | HEX SCH INVERT |
| A7 | 7400 | QAUD NAND |
| A8 | 74LS241 | OCTAL BUFFER |
| A10 | 8214 | PRIORITY ENCOD. |
| | | |
| B1 | 74LS139 | DUAL DECODER |
| B2,3 | 74174 | HEX F/FLOP |
| B4,5 | 8T26 | QUAD BUS TXCVR. |
| B6 | 7400 | QUAD NAND |
| B7 | 74174 | HEX F/FLOP |
| B8 | 7497 | RATE MULT. |
| | | |
| C1 | 7402 | QUAD NOR |
| C2 | 74LS08 | QUAD AND |
| C3 | 74LS00 | QUAD NAND |
| C8 | 74LS158 | DATE SELECTOR |
| C10 | 8214 | PRICRITY ENCOD. |

| LOC | TYPE | DESCRIPTION |
|---|---|---|
| D1 | 74LS273 | OCTAL F/FLOP |
| D2-6 | 2708 | 1K EPROM |
| D7,9 | 2114 | 1K X 4 RAM |
| D10 | 74LS279 | QUAD LATCHES |
| | | |
| E1 | 74LS86 | EX. OR |
| E2 | 74LS00 | QUAD NAND |
| E3 | 555 | TIMER |
| E5 | 7416 | HEX INVT.O.C. |
| E6 | 4N33 | OPTO ISOLATOR |
| E8 | 6850 | ACIA |
| E10 | 74LS138 | DECODER |
| | | |
| F1 | 1488 | QUAD DRIVER |
| F2 | 1489 | QUAD RXCVR |
| F3 | 74LS00 | QUAD NAND |
| F5 | 74LS74 | DUAL F/FLOP |
| F6 | 7403 | QUAD NAND O.C. |
| F8,9 | 6821 | PIA |
| | | |
| VR1 | 7905 | -5V REG. |
| Q1 | BC558 | TRANSISTOR |
| D1 | IN4001 | |

| | RESISTORS | |
|---|---|---|
| R1 | *** | |
| R2 | 4K7 | RP1 |
| R3 | 4K7 | |
| R4-11 | 4K7 | RP1 |
| R12-21 | 4K7 | |
| R22,23 | 1M | |
| R24 | 2K2 | |
| R25,26 | 270R | |
| R27 | *** | |
| R28 | 1K | |
| R29 | 4K7 | |

| | RESISTORS | |
|---|---|---|
| R30 | 4K7 | |
| R31 | 2K2 | |
| R32 | 1K | |
| R33,34 | 5K6 | |
| R35-42 | 4K7 | RP2 |
| R43-50 | 4K7 | RP3 |
| R51-58 | 4K7 | RP4 |
| R59 | 2K2 | |
| R60 | 4K7 | |
| R61 | 4K7 | RP2 |
| R62 | 4K7 | RP3 |

| | CAPACITORS | |
|---|---|---|
| C1,2 | 47UF | 25V ELECT. |
| C3-6 | 220N | |
| C7-9 | 10N | |

| | CAPACITORS | |
|---|---|---|
| 0.01UF | | MONO CERM. |
| 0.1UF | | MONO CERM. |

| | | |
|---|---|---|
| S01 | 10 WAY | HEADER |
| S03 | 26 WAY | HEADER |

| | | |
|---|---|---|
| S02 | 26 WAY | HEADER |

## 14.3 0096 64K RAM CARD

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| A1-A4 | 74LS240 | OCTAL INVERTER |
| A5 | 74LS241 | OCTAL BUFFERS |
| A7 | 74LS373 | OCTAL LATCHES |
| A9 | 74LS132 | QUAD SCH.NAND |
| A11 | 74LS10 | TRIPLE NAND |
| B1 | 74LS174 | HEX F/FLOP |
| B2 | 74LS158 | DATA SELECTORS |
| B3 | 74LS189 | 64 BIT RAM |
| B5-B12 | 4116 | 16K RAM |
| C1 | 74LS14 | HEX SCH.INVT |
| C2 | 74LS30 | BINPUT NAND |
| C3 | 74LS266 | QUAD EX. NOR |

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| D1 | 74LS174 | HEX F/FLOP |
| D2 | 74LS139 | DUAL DECODER |
| D3 | BLANK | |
| D5-D12 | 4116 | 16K RAM |
| E1 | 74LS10 | TRIPLE NAND |
| E2 | 74LS00 | QUAD NAND |
| E3 | 74LS240 | OCTAL INVT. |
| E5-12 | 4116 | 16K RAM |
| F1 | 7404 | HEX INVT. |
| F2 | 74LS240 | OCTAL INVT. |
| F5-F12 | 4116 | 16K RAM |

RESISTORS

| | |
|---|---|
| R1-R5 | 4K7 |
| R6 | 680R |
| R7 | 1K5 |

RESISTOR PACK

| | |
|---|---|
| RP1 | 4K7 |
| RP2,3 | 56R |
| RP4,5 | 100R |
| RP6 | 470R |
| RP7 | 100R |
| RP8 | 470R |
| RP9 | 100R |
| RP10,11 | 470R |

CAPACITORS

0.1UF 50V MONO CERM.
100UF 40V ELECT.

SWITCH

4-IN-LINE

ZENER DIODE

5V1

## 14.4 QFC2 FLOPPY DISK CONTROLLER

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| A1-A3 | 8T97 | HEX TRI-BUFFER |
| A4 | 74LS133 | 13 INPUT NAND |
| A5 | 74LS04 | HEX INVERTERS |
| A6-A8 | 8T97 | HEX TRI-BUFFER |
| A9 | 74LS14 | HEX SCH INVERT |
| B1-B4 | 74LS193 | BINARY COUNTER |
| B5,6 | 74LS75 | QUAD F/FLOP |
| B7,8 | 74LS266 | QUAD EX. NOR |
| B9 | 7404 | HEX INVT. |
| C1 | 74LS174 | HEX F/FLOP |
| C2 | 74LS139 | DUAL DECODER |
| C3 | 74LS08 | QUAD NAND |
| C4 | 74LS174 | HEX F/FLOP |
| C5 | 8T97 | HEX TRI-BUFFER |
| C6.5 | FD1771 | FLOPPY CONTROL |
| C8 | 74LS00 | QUAD NAND |
| C9 | 74LS03 | QUAD NAND O.C. |

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| D1,2 | 74LS74 | DUAL F/FLOP |
| D3 | 74LS37 | QUAD NAND |
| D4 | 74LS139 | DUAL DECODERS |
| D5 | 74LS74 | DUAL F/FLOP |
| D6 | 8T98 | HEX TRI-INVERT |
| D7 | 96S02 | QUAD NOR |
| D8 | 74S74 | DUAL F/FLOP |
| D9 | 74LS74 | DUAL F/FLOP |
| E1 | 9602 | QUAD NOR |
| E2,3 | 74LS02 | QUAD NOR |
| E5 | 74LS00 | QUAD NAND |
| E6 | 74LS10 | TRIPLE NAND |
| E7 | 74S74 | DUAL F/FLOP |
| E8 | 74LS32 | QUAD AND |
| E9 | 74LS08 | QUAD AND |

RESISTORS

| | |
|---|---|
| R1-R3 | 1K8 |
| R5,6 | 10K |
| R7 | 68K |
| R8 | 150R |
| R9,10 | 4K7 |
| R11-R15 | 150R |
| VR1,2 | 5K MULTI TURN |

CAPACITORS

| | |
|---|---|
| C1 | 1UF TAG. |
| C2,3 | 500V STYRO. |
| 0.01UF | MONO CERM. |
| 0.1UF | MONO CERM. |
| 47UF | 25V ELECT. |

REGULATOR 7905 (-5V)

| | |
|---|---|
| 50 WAY | HEADER |
| SW1 | SPDT |

## 14.5 0045 GRAPHICS CARD

| LOC. | TYPE | DESCRIPTION | LOC. | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| A1-A4 | 74LS157 | DATA SELECT. | D1-D3 | 74LS161 | SYNC COUNT. |
| A5 | 74LS133 | 13 INP. NAND | D4 | 74LS14 | HEX SCH.INVT |
| A6 | 74LS14 | HEX SCH.INVT. | D5 | 74LS10 | TRIPLE NAND |
| A7 | 8T28 | BUS XCVR. | D6 | 74166 | SHIFT REGISTER |
| A8 | 8T96 | HEX T.S.TXCVR. | D7 | 33511 | FIFO |
| A9 | 74LS14 | HEX SCH.INVT. | D8 | 74LS00 | QUAD NAND |
| A10 | 74S08 | QUAD AND | D9 | 74S08 | QUAD AND |
| | | | D10 | 9316 | COUNTER |
| B1-B5 | 74LS193 | BINERY COUNT. | | | |
| B6 | 74LS174 | HEX F/FLOP | E1 | 74LS139 | DUAL DECODER |
| B7 | 8T28 | BUS TXCVR. | E2 | 74S11 | TRIPLE AND |
| B8 | 74LS139 | DUAL DECODER | E2.5 | 7404 | HEX INVT. |
| B9 | 74LS10 | TRIPLE NAND | E3 | 74LS86 | QUAD EX. OR |
| B10 | 74S08 | QUAD AND | E5 | 4007 | DUAL COMP.PAIR |
| | | | E8 | 74LS00 | QUAD NAND |
| C1 | 74LS74 | DUAL F/FLOP | E9 | 7404 | HEX INVT. |
| C2,3 | 74LS193 | DUAL DECODER | E10 | 74LS161 | SYNC COUNTER |
| C4 | 74LS393 | DUAL COUNTER | | | |
| C5 | 7404 | HEX INVERTER | F1 | 7409 | QUAD AND O.C. |
| C6 | 93LC8 | OCTAL LATCH | F4 | 96S02 | MONOSTABLE |
| C7 | 9308 | OCTAL LATCH | F6 | 2621N | VIDEO GEN. |
| C8 | 74S74 | DUAL F/FLOP | F7 | 9602 | MONOSTABLE |
| C9 | 74LS08 | QUAD AND | F8 | 74LS74 | DUAL F/FLOP |
| C10 | 7442 | BCD-DEC. CONVT. | F9,10 | 74LS161 | SYNC COUNTER |

| RESISTORS | | RESISTORS | |
|---|---|---|---|
| R1 | 22K | R28 | 10R |
| R2 | 27K | R29 | 120R |
| R3 | 1K | R30 | 68R |
| R4 | 1K | R31 | 470R |
| R5 | 330K | R32 | ** ** |
| R6 | 2K2 | R33 | 68R |
| R7 | 2K2 | R34 | 120R |
| R8 | 10K | R35 | 10R |
| R9 | 12K | R36 | 470R |
| R10 | 4K7 | R37 | 120R |
| R11 | 1MO | R38 | 470R |
| R12 | 10K | R39 | 1K0 |
| R13 | 4K7 | R41 | 100R |
| R14 | 56R | R42 | 1K0 |
| RP1 (R15-22) | 4K7 | R43 | 220R |
| R23 | 470R | R44 | 4K7 |
| RP2 (R24-27) | 4K7 | R45-52 | 1K0 |
| VR1 | 10K MULIT TURN | | |
| VR2 | 2K2 MULTI TURN | | |

CAPACITORS

| | | |
|---|---|---|
| C1-3 | 0.1 | MONO CERM. |
| C4 | 1UF | TAG. |
| C8 | 2N2 | |
| C9 | 33PF | |
| C24 | 33PF | |
| C25 | 33PF | |
| C26 | 4N7 | |
| C27 | 12PF | |
| 0.01UF | 50V | MONO CERM |
| 0.1UF | 50V | MONO CERM |
| 47UF | 25V | ELECT. |

CRYSTAL 3.55MHZ

TRANSISTOR

| | |
|---|---|
| Q1 | BC549 |
| Q2 | BC558 |
| Q3 | 2907 |
| Q4 | 2907 |

REGULATOR

78L05 (+5V)

S01 10WAY HEADER

14.6 0025 16K RAM CARD

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| A1,2 | 8T97 | HEX TRI BUFFER |
| A3,4 | 8T26 | QUAD TRI RXCVR |
| A6,7 | 74S04 | HEX INVERTER |
| B1 | 9321 | DUAL DECODER |
| B2 | 74S08 | QUAD AND |
| B3 | 74174 | HEX F/FLOP |
| B6,7 | 74S00 | QUAD NAND |
| ZD1 | BZX79C5V1 | 5V ZENER |

RESISTORS

| | |
|---|---|
| R1-4 | 1K |
| R5-10 | 270R |
| R11-16 | 27R |
| R17-20 | 1K |
| R21-26 | 330R |
| R27 | 27R |
| R28-31 | 56R |
| R32-37 | 150R |
| R38,39 | 270R |
| R40-43 | 330R |
| R44-47 | 56R |
| R48,49 | 150R |
| R50 | 680R |
| R51 | 4K7 |

CAPACITORS

| | | |
|---|---|---|
| 0.01UF | MONO CERM. | |
| 0.1UF | MONO CERM. | |
| 47UF | 25V | ELECT. |
| 100UF | 35V | ELECT. |

MISCELLANEOUS

| | |
|---|---|
| SW1 | 4 WAY SWITCH |

## 14.7 Q148 LIGHT PEN CARD

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| A1 | LS133 | 13 I/P NAND |
| A2 | LS04 | HEX INVERT. |
| A3 | LS174 | HEX F/FLOP |
| A4,5 | 8T26 | QUAD BUS TXCVER |
| A6 | LS14 | HEX SCH.INVERT. |
| A7 | LS295 | SHIFT REGISTER |
| A8 | LS74 | DUAL F/FLOP |
| | | |
| B1 | LS04 | HEX INVERT. |
| B2 | LS139 | DUAL MULTIPLEX |
| B3 | LS295 | SHIFT REGISTER |
| B4 | 6840 | TIMER |
| B6 | 6821 | PIA |
| B7 | LS295 | SHIFT REGISTER |
| B8 | LS161 | BINARY COUNTER |
| | | |
| Q1 | 2N2369 | TRANSISTOR |
| Q2,3 | BC108 | TRANSISTOR |

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| C1 | LS04 | HEX INVERT. |
| C2 | LS10 | TRIPLE NAND |
| C3,7 | LS295 | SHIFT REGISTER |
| C8 | LS161 | BINARY COUNTER |
| | | |
| D1 | LS02 | QUAD NOR |
| D2 | LS86 | QUAD EXCL.OR |
| D3 | LS393 | DUAL COUNTER |
| D4 | LS161 | BINARY COUNTER |
| D5,6 | LS266 | QUAD EXCL.NOR |
| D7,8 | LS153 | DUAL MULTIPLEX. |
| | | |
| E1 | LS00 | QUAD NAND |
| E2 | LS74 | DUAL F/FLOP |
| E3 | LS221 | DUAL MONO |
| E4 | LS04 | HEX INVERT. |
| E5 | LS00 | DUAL NAND |
| E6 | LS74 | DUAL F/FLOP |
| E7 | LS14 | HEX SCH.INVERT. |
| E8 | LS153 | DUAL MULTIPLEX. |

| | RESISTORS |
|---|---|
| R1 | 2K2 |
| R2 | 2K7 |
| R3-6 | 100R |
| R7,8 | 10K |
| R9 | 2K2 |
| R10 | 120K |
| R11 | 10K |
| R12 | 2K2 |
| R13 | 1K |
| R14 | 1M |
| R15 | 220K |

| | RESISTORS |
|---|---|
| R16 | 680R |
| R17 | 10K |
| R18 | 1M |
| R19 | 330R |
| R20 | 220R |
| R21 | 330R |
| R22 | 220R |
| R23 | 470R |
| R24-28 | 4K7 |
| R29 | 100R |

| | CAPACITORS |
|---|---|
| C1-4 | 150PF |
| C5,6 | 1NF |
| C7 | 100N |
| C8 | 1UF TAG. |
| C9 | 150PF |

| | CAPACITORS |
|---|---|
| C10-13 | 100N |
| C14 | 22UF |
| C15 | 470PF |
| C16 | 100PF |
| 0.01UF | MONO CERM. |
| 0.1UF | MONO CERM. |
| 47UF 25V | ELECT. |

| | MISCELLANEOUS |
|---|---|
| SO1 | 10 WAY HEADER |

14.8 CMI Ø2 MASTER CARD

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| A1 | LS133 | 13 I/P NAND |
| A2,3 | LS14 | HEX INVT. SCH. |
| A4 | LS174 | HEX F/FLOP |
| A5 | 8T26 | QUAD BUS TXCVR. |
| A6 | 6840 | TIMER |
| A7 | LS367 | HEX BUS DRIVER |
| A8 | LS14 | HEX INVT. SCH. |
| A9 | 7611 | ROM |
| A10 | LS00 | QUAD NAND |
| B1 | LS21 | DUAL 4 I/P AND |
| B2 | LS00 | QUAD NAND |
| B3 | LS10 | TRIPLE NAND |
| B4 | LS138 | DECODER |
| B5 | 8T26 | QUAD BUS TXCVR. |
| B7 | S175 | QUAD F/FLOP |
| B8 | 7611 | ROM |
| B9 | 6821 | PIA |
| B10 | LS00 | QUAD NAND |
| C1 | LS74 | DUAL F/FLOP |
| C2 | LS02 | QUAD NOR |
| C3 | LS11 | TRIPLE AND |
| C4 | LS00 | QUAD NAND |
| C5,7 | LS373 | OCT. LATCH |
| C8 | 8214 | PRIORITY ENCOD. |
| C10 | 7497 | RATE MULT. |

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| D1 | LS03 | QUAD NAND O.C. |
| D2 | LS123 | DUAL MONO STAB. |
| D3 | LS74 | DUAL F/FLOP |
| D4 | LS138 | DECODER |
| D9 | LS02 | QUAD NOR |
| D10 | 7497 | RATE MULT. |
| E1 | 4051 | MULTIPLEXER |
| E2 | LS14 | HEX INVT. SCH. |
| E3 | 741 | OP AMP |
| E4 | AD7523 | A-D CONVT. |
| E5 | 6821 | PIA |
| E7 | 3140 | FET OP AMP |
| E8 | LS161 | COUNTER |
| E9 | AD583 | S/HOLD |
| E10 | S74 | DUAL F/FLOP |
| F1,5 | 4051 | MULTIPLEXER |
| F7,8 | 4051 | MULTIPLEXER |
| F10 | 4051 | MUITIPLEXER |
| | MISCELIANECUS | |
| Q1 | 2N2369 | |
| ZD1,2 | 5V6 | |
| D1,2 | 1N4004 | |
| D3,4 | 1N914 | |
| D5 | MBR120P SCHOTTKY | |
| L1 | 1UH CHOKE | |
| L2 | FERRITE BEAD | |
| CRST. | 34.2917MHZ | |
| 10 WAY | HEADER | |

| | RESISTOR | | RESISTOR | | RESISTOR |
|---|---|---|---|---|---|
| P1 | 4K7 | R39 | 180K | R63 | 22K |
| R2 | 56P | R40 | 56K | R64 | 39K |
| R3-12 | 4K7 | R41 | 3K9 | R65 | 68 K |
| R13 | 180R | P42 | 5K6 | R66 | 150K |
| R14 | 22K | R43 | 8K2 | R67 | 12K |
| R15-18 | 56R | R44 | 12K | R68 | 680R |
| P19 | **** | R45 | 18K | R69 | 1K |
| R20 | **** | R46 | 33K | R70 | 1K5 |
| R21 | 5K6 | R47 | 56K | R71 | 1K8 |
| R22 | 100K | R48 | 180K | R72 | 3K3 |
| R23 | 100R | R49 | 56K | R73 | 5K6 |
| R24 | 150K | R50 | 3K9 | R74 | 10K |
| P25 | 5K6 | R51 | 5K6 | R75 | 22K |
| R26 | 4K7 | R52 | 8K2 | R76 | 3M3 |
| R27 | 100K | R53 | 12K | R77 | 180K |
| R28 | 1K | R54 | 18K | R78 | 270K |
| R29-30 | 10K | R55 | 33K | R79 | 390K |
| R31 | 56K | R56 | 56K | R80 | 560K |
| P32 | 3K9 | R57 | 180K | R81 | 820K |
| R33 | 5K6 | R58 | 82K | R82 | 1M5 |

| | | | | | |
|---|---|---|---|---|---|
| R34 | 8K2 | R59 | 4K7 | R83 | 2M7 |
| R35 | 12K | R60 | 6K8 | R84 | 4M7 |
| R36 | 18K | P61 | 10K | R85 | 10K |
| R37 | 33K | R62 | 15K | R86-87 | 680R |
| R38 | 56K | | | | |
| RP1 | 10K | | | | |

| CAPACITORS | | | CAPACITORS | |
|---|---|---|---|---|
| C1 | 56P | | C10 | 47N |
| C2,3 | 47UF | | C11 | 100P |
| C4,5 | 680P | | C12 | 47N |
| C6 | 10N | | C13 | 180P |
| C7 | 1N | | C14 | 47N |
| C8 | 12UF | | C15 | 100P |
| C9 | 6N8 | | C16 | 47N |
| 0.01UF | | MONO CERM. | 47UF | 25V ELECT. |
| 0.1UF | | MONO CERM. | | |

14.9 CMI01 CHANNEL CARD

********** NOT AVAILABLE ********

## 14.10 CMI 04 AUDIO CARD

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| IC1-4 | 4136 | QUAD OP AMP |
| IC5-10 | 301 | OP AMP |
| IC11 | *** | |
| IC12 | 541 | AMP |
| IC13 | 7815 | REG. 15V |
| IC14 | 7915 | REG.-15V |
| IC15 | 741 | OP AMP |
| | CAPACITORS | |
| C1,2 | 100N | |
| C3 | 100UF | |
| C4 | 390P | |
| C5 | 100UF | |
| C6 | 100N | |
| C7 | 100UF | |
| C8 | 100N | |
| C9 | 100UF | |
| C10 | 100N | |
| C11 | 6.8UF | |
| C12 | *** | |
| C13 | 10N | |
| C14 | 100N | |
| C15 | 4P7 | |
| C16 | 6.8UF | |
| C17 | 100N | |
| C18-35 | 6.8UF | |
| C36,37 | 33P | |
| C38,39 | 6.8UF | |
| | RESISTORS | |
| R1 | 10K | |
| R2 | 56K | |
| R3 | 100K | |
| R4 | 1K | |
| R5 | 56K | |
| R6 | 4R7 | |
| R7 | 100R | |
| R8-23 | 330R | |
| R24 | 2K2 | |
| R25 | 5K6 | |
| R26-28 | 10K | |
| R29 | 2K7 | |
| R30 | 5K6 | |
| R31-33 | 10K | |
| R34 | 2K7 | |
| R35 | 5K6 | |
| R36-38 | 10K | |
| R39 | 2K7 | |
| R40 | 5K6 | |
| R41-43 | 10K | |
| R44 | 2K2 | |
| R45 | 5K6 | |

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| | TRANSISTORS | |
| Q1 | 2N3055 | |
| Q2 | 2N2955 | |
| Q3-6 | EC109 | |
| Q7 | 2N3638 | |
| Q8 | 2N3643 | |
| | MISCELLANEOUS | |
| D1,2 | 1N4001 | |
| ZD1-3 | 3V9 | |
| RELAY | NF2 12V | |
| FUSE | 2A SLO BLO | |
| | CAPACITORS | |
| C40 | 10P | |
| C41 | 33P | |
| C42 | 12P | |
| C43 | 6.8UF | |
| C44 | 33P | |
| C45 | 47UF | |
| C46 | 3P3 | |
| C47 | 1N | |
| C48 | 1UF | |
| C49 | 100N | |
| C50 | 100UF | |
| | RESISTORS | |
| R64-71 | 2K7 | |
| R72,73 | 10K | |
| R74 | 1K2 | |
| R75,76 | 330R | |
| R77 | 10K | |
| R78 | 22K | |
| R79 | 1K | |
| R80 | 680R | |
| R81,82 | 10K | |
| R83 | 680R | |
| R84,85 | 330R | |
| R86 | 2K2 | |
| R87-89 | 10K | |
| R90-93 | 680R | |
| R94 | 100K | |
| R95 | 2K2 | |
| R96 | 100K | |
| R97 | 33K | |
| R98 | 1K | |
| R99 | 2K2 | |
| R100-3 | 10K | |
| R104 | 1K | |

| | |
|---|---|
| R46-48 | 10K |
| R49 | 2K7 |
| R50 | 5K6 |
| R51-53 | 10K |
| R54 | 2K7 |
| R55 | 5K6 |
| R56-58 | 10K |
| R59 | 2K7 |
| R60 | 5K6 |
| R61-63 | 10K |

| | |
|---|---|
| R105 | *** |
| R106 | *** |
| R107 | 56K |
| R108 | 56R |
| R109 | 2K2 |
| R110 | 270R |
| R111-8 | 5K6 |

## 14.11 CPSA REGULATED POWER SUPPLY

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| Q1,2 | ASZ15 | POWER TRAN. |
| Q3-6 | 2N3055 | POWER TRAN. |
| Q7 | MJ4502 | POWER TRAN. |
| ZD1 | BZX79 | 5V6 ZENER |
| ZD2 | 1N5339 | 5V6 ZENER |
| | RESISTORS | |
| R1 | 0.012 | |
| R2 | 3R3 | 5W |
| R3-6 | 10R | 1W |
| R7-11 | 0.22R | 5W |
| | CAPACITORS | |
| C5 | 680 | UF ELECT. |
| C6 | 47 | UF ELECT. |
| C7 | 4700 | UF ELECT. |
| C8 | 47 | UF ELECT. |
| C9 | 1 | UF TANT. |
| C10 | 1 | UF TANT. |
| C11 | 0.1 UF | |
| FS1 | PK15 | 15A FUSE |

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| IC1 | 7805 | 5V REG. |
| IC2 | 7824 | 24V REG. |
| IC3 | 7812 | 12V REG. |
| IC4 | 7912 | -12V REG. |
| SCR1 | IR30B | |
| | RESISTORS | |
| R12 | 330R | |
| R13 | 3R3 | 5W |
| R14 | 0.51 | 5W |
| | CAPACITORS | |
| C12 | 22 | UF TANT. |
| C13 | 0.1 | |
| C14,15 | 100 | UF ELECT. |
| C16 | 0.01 | |
| C17,18 | 47 | UF ELECT. |
| C19 | 0.1 | |

## 14.12 C236 FRONT PANEL CONTROL CARD

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| IC1 | 14411 | BAUD RATE GEN. |
| IC2 | IS14 | HEX SCH.INVERT. |

**RESISTORS**

| | |
|---|---|
| R1,2 | 270R |
| R3 | 8K2 |
| R4 | 18R |
| R5 | 560R |
| R6 | 100R |
| R7 | 1M |

**CAPACITORS**

| | | |
|---|---|---|
| C1,2 | 10N | |
| C3 | 47UF | ELECT. |

| | |
|---|---|
| CRYST. | 1.8432MHZ |
| S01 | 25 WAY CABLE CONECTOR |

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| L1,3 | LED | YELLOW |
| L4,5 | LED | RED |

**SWITCHES**

| | | |
|---|---|---|
| SW1 | 8125 | SPDT |
| SW2 | 7211 | DPDT |
| SW3 | 8125 | SPDT |
| SW4 | 7211 | DPDT |
| SW5 | 7101 | SPDT |
| SW6 | 7101 | SPDT |
| SW7 | 7101 | SPDT |
| SW8 | 8 POS. | ROTARY |
| SW9 | 8 WAY | IN-LINE |

# FAIRLIGHT

# COMPUTER MUSICAL INSTRUMENT

# DISC DRIVE SERVICE MANUAL

Revision 1.0

July 1982

CmI

Fairlight Instruments Pty Ltd

CONTENTS

## 1. Introduction

Each CMI has two YE-Data YD-174 8-inch floppy disc drives installed as standard equipment. The left hand drive, as viewed from the front of the CMI, is referred to as Drive 0 and normally contains the CMI System Disc which is used to boot the system during restart. The right hand drive, Drive 1, contains the user's work disc.

This document contains information pertaining to the installation and removal of disc drives, set-up and alignment of new drives, preventative and basic corrective maintenance, and disc system fault diagnosis.

## 2. Removal and Installation of Disc Drives

(Refer to drawing DMC001)

YD-180 sur les 2 X.

To remove either or both YD-174 units, first remove the top bottom, and rear panels of the CMI according to the mainfram disassembly procedure. Then perform the following procedure:

(1) Carefully up-end the CMI so that it rests on its left hand end, on a non-scratching surface.

(2) Remove the 50-way flat cable from the rear of both drives.

(3) Remove the 3-way AC power connector and the 6-way DC power connector from the rear of both drives.

(4) Each drive is supported in the CMI mainframe by four screws (item 25 in DMC001). Two of these pass through the top aluminium panel (13) and the other two pass through the bottom panel (14). Remove these screws and slide the disc drive out through the front.

Installation of a YD-174 unit is the reverse process.

DISC
DISC
DI

DISK DRIVE OPTIONING

On the Disk drive Printed Circuit Board there are two items which must be located.

Looking at the P/C Board component side, on the Top Left Hand corner is the serial number, just to the left are some option pins marked DS1 DS2 DS3 DS4
These are the D/Drive position numbers

Near the 50 Way connector there are two sockets which appear at right angles to most of the IC,s.In these sockets are terminating resistors for the 50 Way signal cable in the form of an IC marked Beckman 899-3-R150.
NOTE: On the C.M.I the D/Drive closest the center is known as Drive 0 and the other closest the right hand side is known as Drive 1.

DRIVE )0
1. shorting lug should be on DS1
2. Terminating Resistors should be removed.
DRIVE 1
1. Shorting lug should be DS2
2. Terminating Resistors should be in.

## 3. Disc Drive Set-up and Alignment

### 3.1 Pre-alignment Set-up

(1) Check that 115V motor is fitted. All CMI's use 115V drives. The CMI power supply may be switched to allow for different local mains voltages.

(2) Check that the correct pulley for the local mains frequency is fitted. 50Hz pulleys have a red identification mark, while 60Hz pulleys are marked green.

(3) Link 'Y' at location G4 on the disc drive p.c.b. (see Fig. 4.6)

(4) Link 'C', level with row E near the edge connector on the disc drive p.c.b.

(5) For drive 0, link DS1 on p.c.b. For drive 1, link DS2. Both links are level with row I.

(6) Remove link block package at E1 and open circuit links 'X' and 'Z' (break legs off link block package).

(7) Reinstall link block

(8) Check that ~~one drive~~ DRIVE 1 (right hand drive) in the CMI, but not both, has two 150 ohm termination resistor packs installed alongside the edge connector.

### 3.2 Disc Drive Alignment

New disc drives require the radial alignment of the read/write head and the track zero sensor to be checked to account for any maladjustments which may occur during shipping. This requires a special Radial Alignment Disc, (Fairlight Part No G0706 plus the Fairlight Disk Diagnostic Disk containing the test program 'DSKTST'.

#### 3.2.1 Radial Alignment

(1) Place the drive on its side, with the main drive motor towards the bottom.

(2) Connect an oscilloscope (CRO) as follows to the block of test pins marked "TP" near the centre of the YE Data p.c.b. (see fig. 4.6):

| Pin | CRO |
|---|---|
| A | Channel A |
| B | Channel B |
| 3 | Ext trig |

(3) Set the CRO as follows:
Inputs on AC
trig on external negative
time base to 20 mS/div

add channels A and B
invert one channel
vertical sensitivity to 100mV/div

(4) Load a disc containing the test program DSKTST and run it by typing DSKTST<CR>.

(5) Type
RA,D,S<CR> where D = drive number (0 or 1)
S = side number (0 or 1)

(6) Insert Alignment Disc and hit a key. This steps the head to track 38.

(7) A "double eye" pattern should appear on the CRO. The amplitudes of the two lobes must be within 70% of each other.

(8) If side 0 is acceptable, repeat test for side 1

(9) If either side requires adjustment, loosen the two Philips head screws which clamp the head carriage assembly to the steel stepper motor belt. The screws are accessed through two holes in the side of the drive chassis.

(10) Gently tap the carriage assembly or move the belt by hand until the lobes are within 70% amplitude with the screws retightened (tightening the screws tends to change the lobe pattern), for both sides of the disc.

(11) Hit ESC to terminate the radial alignment test.

### 3.2.2 Track Zero Sensor Test

After the head is radially aligned, the track 00 sensor should be checked.

(1) Still running DSKTST, type
T0,D where D = drive (0 or 1)

(2) Insert a scratch disc and hit any key.

(3) T0 causes the head to oscillate between track 00 and track 01. Monitor the sensor signal at pin B12 of the J2 connector block on the drive p.c.b. It should oscillate with movement of the head.

(4) Terminate test by hitting ESC

## 4. Disc Drive Maintenance

Under normal circumstances preventive maintenance is no required on the YD-174. If severely dirty environments ar encountered, an occasional cleaning of the drive may be performe to assure continued reliable performance.

Only basic corrective maintenance is documented here. If is determined that a disc drive requires more extensive repairs than are described in this section, return the unit to Fairligh Instruments for service. This document should provide sufficien information to determine whether return of the unit is necessary

### 4.1 Preventive Maintenance

Under normal circumstances preventive maintenance is no required on the YD-174. If severely dirty environments ar encountered, an occasional cleaning of the drive may be perform to assure contiued reliable performance.

#### 4.1.1 Visual Check

Visual inspection is the first step in any maintenan operation. Always look for corrosion, dirt, wear, binds, a loose connections. Noticing these items may save downtime later

#### 4.1.2 Cleaning

Cleanliness cannot be overemphasized in maintenance of t YD-174.

Caution: The head/carriage assembly is a factory-adjusted a tested assembly. Do not try to adjust or repair this intern component. Do not, for any reason, clean the read/write head To do so would cause severe damage to the head surfaces or he spring supports.

| Parts | Observe | Procedure |
|---|---|---|
| 1. Main Frame | Inspect for loose screws, connectors, switcnes, etc. | Clean main frame |
| 2. Drive Belt | Frayed or weakened area | Change new belt |

## 4.2 PCB Removal and Replacement

1. Disconnect all connectors (J1, J2, J3, J5) from PCB.
2. Remove two mounting screws near the J1 connector and loose two screws on the J2 edge of the PCB.
3. Slide PCB away from stepper and remove it.
4. Reverse the procedure for replacement.

## 4.3 Index Lamp Assembly

### 4.3.1 Service Check

1. Turn on power.
2. Verify voltage of 2.0 to 3.4 V between "J2-B8" and "GND" test points on PCB.

### 4.3.2 Removal and Replacement

1. Disconnect J2 connector from PCB.
2. Remove two lamp leads from J2 connector by pushing down on tabs with a tweezer (BLACK to J2-A8, RED to J2-B8).
3. Remove cable clamp and lamp cable.
4. Remove two mounting screws and lamp assembly.
5. Reverse the procedure for replacement.

Note: When installing the assembly, align the pointer of la assembly with the timing line of index sensor assembly a tighten two mounting screws by pushing lamp assembly again carrier stop away from the front door.

Caution: Make sure the locking tabs on the terminals engage the connector slot to prevent the leads from pushing out wh plugged in.

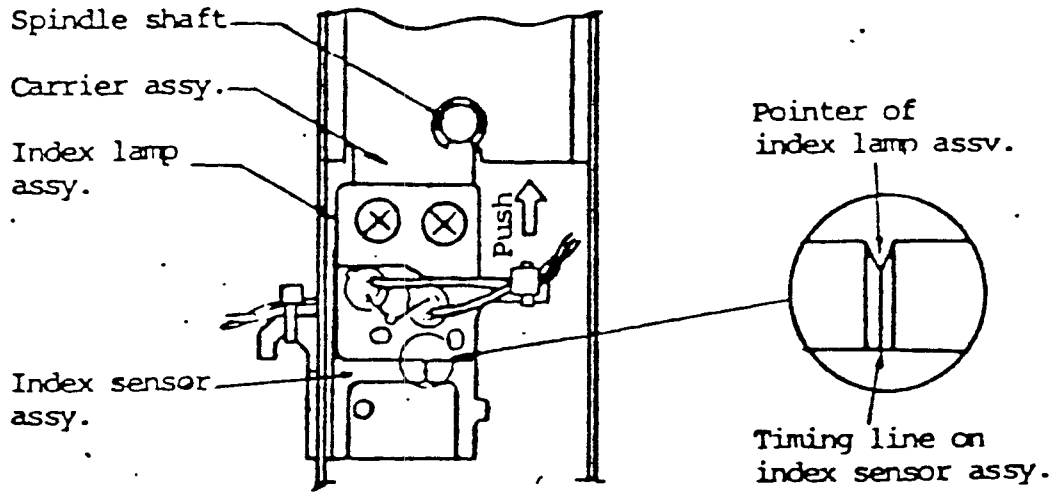



Fig. 4.1 Index Lamp Assembly

## 4.4 Index Sensor Assembly

### 4.4.1 Service Check

1. Turn on power.
2. Verify the voltage of 4 to 5.25 V when disc door is closed without a Diskette, and 0 to 0.3 V when a Diskette is inserted backwards and door closed, between "J2-A7" and " GND " test points on PCB.
3. Repeat the same procedure between "J2-A6" and " GND " test points on PCB.
4. Remove the Diskette.

### 4.4.2 Removal and Replacement

1. Disconnect J2 connector from PCB.
2. Remove four SENSOR leads from J2 connector by pushing down on tabs with a tweezer. (BLACK to J2-A7 RED to J2-B7, BLUE to J2-A6, ORANGE to J2-B6)
3. Remove screw, washer and assembly.
4. Reverse the procedure for replacement.

Note: When installing assembly, push it away from its cable, against the main frame stop.

Caution: Make sure that the locking tabs on the terminals engage in the connector slot to prevent the leads from pushing out when plugged in.

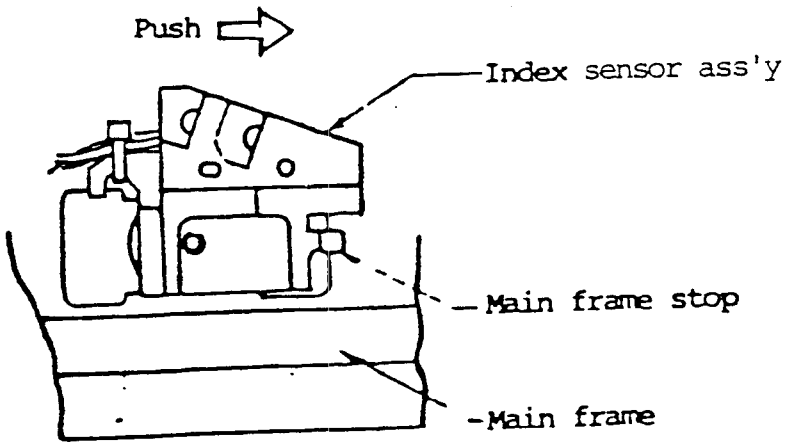



Fig 4.2 Index sensor assembly

## 4.5 Track 00 Sensor Assembly

### 4.5.1 Service Check

1. Position the head/carriage by hand to its limit away from spindle (the outer edge of TRACK 00).
2. Turn on power.

Note: This positions head/carriage to TRACK 00.

3. Verify voltage of 1.0 to 1.7 V between "J2-B12" and " GND " test points on PCB without a Diskette.
4. Verify voltage of 0 to 0.3 V between "J2-A11" " GND " test points on PCB.
5. With power off, move the head/carriage by hand toward spindle, 4 stepper detent positions. (TRACK 04)
6. With power on, verify voltage of 4.0 to 5.25 V between the same test points in step 4.

### 4.5.2 Removal and Replacement

1. Disconnect J2 connector from PCB.
2. Remove four leads from J2 connector by pushing down on tabs with a tweezer. (BLUE to J2-A12, ORANGE to J2-B12, BLACK TO J2-A11, RED to J2-B11).
3. Remove the mounting screw and assembly.

Note: When installing assembly, insert its two pins into main frame holes and tighten mounting screw.

Caution: Make sure that the locking tabs on the terminals engage in the connector slot to prevent the leads from pushing out when plugged in.

## 4.6 Write Protect Sensor Assembly

### 4.6.1 Service Check

1. Turn on power.
2. Verify voltage of 1.0 to 1.7 V between J2-B14 and " GND " test points on PCB without a Diskette.
3. Verify voltage of 4 to 5.25 V when door is closed and 0.03 V when a Diskette without a write protect notch is inserted and the door closed, between "J2-A13" and " GND " test points on PCB.
4. Remove the Diskette.

### 4.6.2 Removal and Replacement

1. Disconnect J2 connector from PCB.
2. Remove four leads from J2 connector by pushing down on tabs with a tweezer. (BLUE to J2-A14 ORANGE to J2-B14 BLACK to J2-A13 RED to J2-B13)
3. With door open, remove the bail mounting screw, washer and bail. (Refer to section 4.7)

4. Remove the mounting screw and assembly.
5. Reverse the procedure for replacement.

Note: When installing assembly, insert its pin into the mai frame hole and tighten the mounting screw.

Caution: Make sure that the locking tabs on the terminals engag in the connector slot to prevent the leads from pushing out whe plugged in.

### 4.7 Bail Assembly, Removal and Replacement

Caution: The read/write heads must not be allowed to com together without a piece of clean paper inserted between the hea surfaces.

1. Insert a piece of clean paper between the head surfaces.
2. Remove the bail mounting screw and washer.
3. Remove bail assembly, pulling away from solenoid.
4. Reverse the procedure for replacement.

Note: Check that the plunger may be moved when pushing it fro the side.

Caution: When installing the bail assembly, make sure that it i placed under the carriage arm tab.

### 4.8 In Use Led, Removal and Replacement

1. Disconnect J2 connector from PCB.
2. Remove two leads from J2 connector by pushing down on tab with a tweezer. (BLACK to J2-A15 RED to J2-B15)
3. Remove LED holder and LED.
4. Reverse the procedure for replacement.

## 4.9 Steel Belt Wiper, Removal and Replacement

1. The belt dustseal cover is obscured by the pop-up assembl which ejects the disc when the door is opened. With doo open, remove the two mounting screws on the pop-up assembl and the assembly itself.
2. Remove the two cover retaining screws and dustseal cover.
3. Remove wiper from dustseal cover.
4. Reverse the procedure for replacement.

Note: When installing a new wiper into dustseal cover, push against the cover stop toward the arrow direction on cover.

Caution: When installing dustseal cover on stepper, align th dustseal cover so that wiper may slightly touch steel bel between head/carriage and pulley.

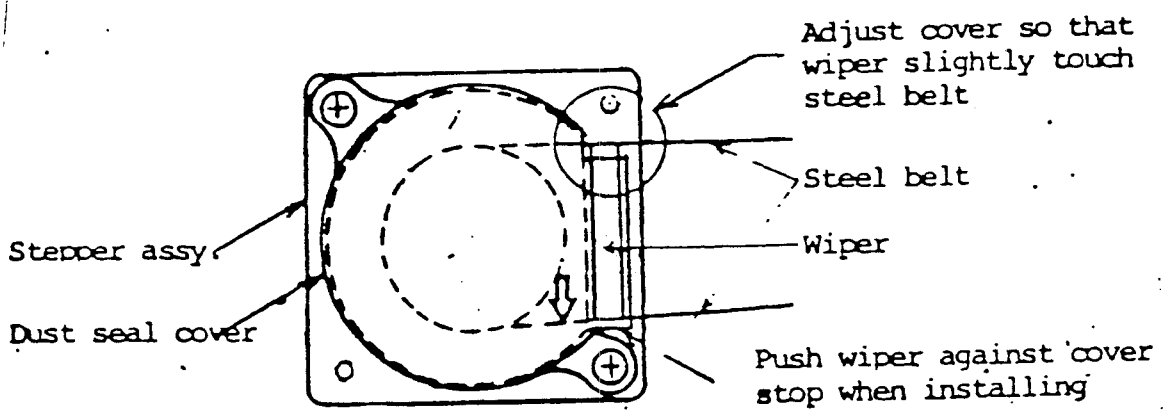



Fig. 4.3 Steel Belt Wiper

## 4.10 Drive Belt and Pulley, Removal and Replacement

1. Remove PCB. (Refer to section 4.2)
2. Remove belt.
3. Loosen pulley setscrew and remove pulley from motor shaft.
4. Reverse the procedure for replacement. Align the setscrew with the flat surface of motor shaft.

Note: Check that the surface of the pulley is aligned with the end of the motor shaft.

Note: Check that the belt is riding on the center of the spindle pulley and drive pulley, rotating spindle pulley counterclockwise by hand.

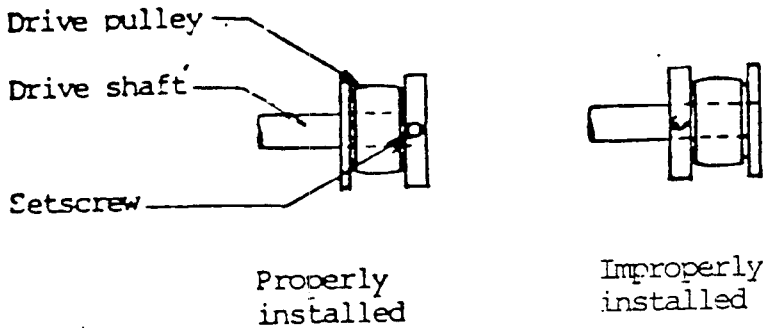



Fig. 4.4 Drive Pulley

## 4.11 Drive Motor Assembly, Removal and Replacement

1. Remove PCB (refer to section 4.2) and drive belt (4.10)
2. Loosen pulley setscrew and remove setscrew from motor shaft.
3. Remove AC connector from connector clamp by pushing down on latch.
4. Remove the two screws which hold the capacitor clamp to the disc drive body.
5. Remove the three screws securing the drive motor and withdraw the motor.
6. Reverse the procedure for installation.

Note: When installing the motor, push it toward the front door and the AC connector clamp against two main frame stops.

Note: Make sure the ground lead is installed on the capacitor clamp.

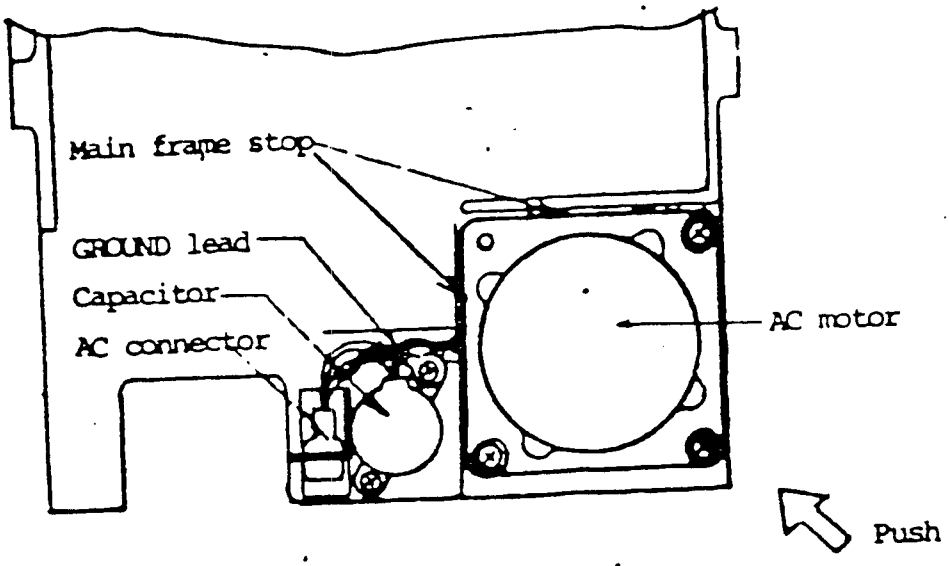



Fig 4.5 Drive Motor and Capacitor

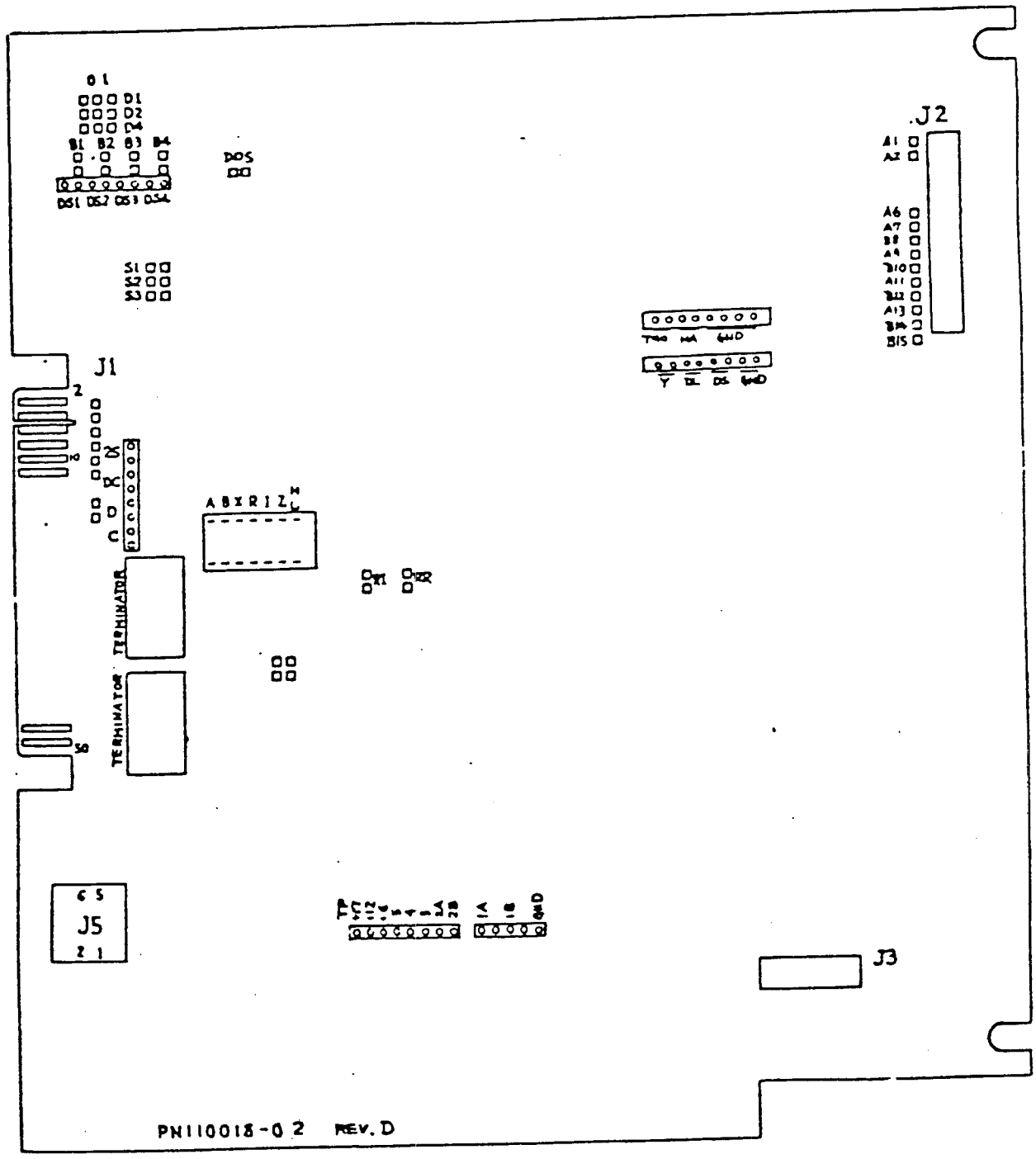



Fig. 4.6 PCB Test point and Connector Locations

## 5. Floppy Disc System Diagnosis

The CMI Floppy Disc System comprises the QFC-2 Floppy Disc Controller as well as the disc drives themselves. The first step in servicing a CMI with an apparently faulty disc system is to establish in what subassembly the fault actually lies.

The general procedure to follow in disc system fault tracing is:

(1) Check all disc system cables, especially the 50 way flat cable for open circuits or shorts and ensure all connections are secure.
(2) Use the system test program CHECK to determine if the fault is in the drive itself (or the diskette) or the disc controller/DMA data transfer system.
(3) If the disc drive is faulty, use DSKTST to further analyse the fault.
(4) Otherwise, refer to the CMI Mainframe manual to trace the fault in the QFC-2 controller.

### 5.1 Test Program CHECK

Allows checking of

- Cyclic Redundancy Check (CRC) errors
- Data transfer between memory and disc
- RAM bit corruption errors

Command Syntax

CHECK <UNIT>,<HEXNUM>;<OPTIONS>

<UNIT>::=<COLON><NUMBER>

<HEX NUMBER>::=<HEX DIGIT>|<HEX DIGIT>

<HEX DIGIT>::=<NUMBER>|A|B|C|D|E|F

<NUMBER>::=1|2|3|4|5|6|7|8|9|0

(1) Disc Integrity Check

Options: none required

This is the default CHECK routine. Entire disc in specified drive is read to check for CRC errors.

(2) Read Data D.M.A. Verify

Option: V

Reads entire disc in specified drive twice, into

separate blocks of memory and verifies data against itself.

(3) Write Data D.M.A. Verify

Options: W,D (May be used together)

The W option creates a file, writes distinctive data to each sector of the file and reads each sector of the file back, twice, into different areas of memory for verification. All unfree disc space will be allocated to the file.

The D option is a destructive (to the disc contents) test which writes a unique "ADD -29" pattern to each sector in an interleaved fashion, reads it back, and verifies the data.
Interleaving of blocks ensures track boundaries are continually being crossed. A delay can be introduced using the "T" option (see below) to isolate head-load timing problems.

(4) Other Options

| Option | Use with | |
|---|---|---|
| R | W | use random number pattern instead of "29" pattern |
| P=XX | W | use pattern XX where XX = <he |
| number> | | write the pattern to disc, read back and verify |
| E=XX | all | print error if total recover-able disc errors exceed XX where XX = <hex number>. Default value is 0. |
| T=XX | all | delay XX*10 ms. after |
| read/write | | where XX = <hex number> |
| C | all | test continously alternating between 'add-29' and a random number pattern |
| L | all | all error messages printed c |
| printer | | |

(5) Error messages

(a) Disc Read/Write Errors
These are of the form

**PROM I/O ERROR -- STATUS = <status byte> AT h DRIVE i - PSN j

where h is not significant
i = drive number
j = physical sector number at which the error occurred
and the status byte can be interpreted as follows:

31 data C.R.C. error
32 disc is write protected
33 disc is not ready for some reason
34 deleted data address mark read
35 abnormal command termination
36 invalid sector address
37 seek error (track not found)
38 data mark read error
39 address mark read error

(b) Verify Errors
When a verify error is encountered the offending disc sector is re-read into the QDOS sector buffer and matched against system RAM to determine where the error came from. The program then reports the corresponding address in RAM, the data expected, the erroneous data, the physical sector number of the disc where the error occured, and the byte offset within the sector.

(6) Termination

Test is terminated by -
ESC key (sets system error status word)
More then 20 errors logged
User supplied iteration counter expired (default 1)

System error status word will be set if any error condition has been reported.

## 5.2 Test Program DSKTST

DSKTST comprises five main test routines and a number of utility commands. The main routines are as follows -

| | |
|---|---|
| #1 Write/read test | (destructive) |
| #2 Read C.R.C. test | (non-destructive) |
| #3 Worst case seek test | (non-destructive) |
| #4 Worst case data pattern R/W | (destructive) |
| #5 Sector/drive uniqueness | (destructive) |

Tests can be run separately or in destructive/non-destruct groups by typing as follows -

DN,(0 or 1 or B) [,X]<CR> (Do all non-destruct tests)

DD,(0 or 1 or B) [,X]<CR> (Do all destructive tests)

ST#<tests>,(0 or 1 or B)[,X]<CR>
where <tests> = up to 10 test numbers separated by '-'

The extended test option X accumulates error counts over a number of passes.

ESC key will abort test in progress

Typing OS<CR> will return the user to QDOS and reboot th system.

Examples: DN,0<CR> does all non-destructive tests c drive 0 only.

ST#1-3-5,B,X does tests 1,3 and 5 on both drive with error count accumulation.

If stop on error option is selected (in answer to a prompt) the user may choose -

C continue
L loop
R reset stop on error

if an error stop occurs.

Error Reporting

Error printouts take the following form :-

<drive no.> <error type> <track no> /<physical sector no> <*>

Presence of '*' indictes a "hard" disc error
e.g. 1 E3 1F /0325 *
means :- drive no 1
error type 3 (E3)
track no 1F
p.s.n 0325
error was not recoverable on retry (*)

If after three retries the error persists, it will be logged as a hard error (indicated by *).

Error types are as follows (per QDOS ROM codes) :-

E1 data CRC error
E2 disc is write protected
E3 disc is not ready for some reason
E4 deleted data address mark read
E5 abnormal command termination
E6 invalid sector address
E7 seek error (track not found)
E8 data mark read error
E9 address mark read error

Additional error types are :-
E@ data read back is not the same as data written

Additional error types from the drive uniqueness test are :-

EA body of data buffer is not zero after test data
EB unique data for this drive/sector is incorrect.

Error Graphs

Errors may be summarised by use of the 'PG' command. This summary plots the track no. as the vertical ordinate and the number of errors as the horizontal ordinate.

A horizontal line may contain up to 11 error types (codes) with each character representing (n*horizontal scale) errors.

The error graph is divided into two blocks. The left hand block relates to drive 0 errors, the right hand block to drive 1.

The graph is printed starting at the first track with errors logged and finishes with the last track with errors logged.

To stop the display rolling off the screen, <control W> can be used to stop printing. Subsequent carriage returns will print a little at a time, an escape will terminate the 'PG', and any other character will resume continuous printin

In the case of double sided systems, each disc 'cylinder' is considered as two tracks, so even track numbers correspon to side 0 of the disc and odd track numbers correspond to side 1.

Utility Commands

Commands for utility programmes are as follows

| | |
|---|---|
| HD,d,hhhh | Head load timing test on drive d at speed hhhh (100 mS = D8F0) |
| IX,d | Index sensor alignment test on drive d. t1=tk 1. t2=tk 76. |
| AT,d,s | Read data amplitude test on drive d. s is optional side select (0 or 1). t1=tk 0. t2=tk 76. |
| RA,d,s | Radial alignment test on drive d. s is optional side select (0 or 1) t1=0-38. t2=77-38. t3=39-38. t4=37-38. |
| AZ,d,s | Head azimuth test on drive d. s is optional side select. t1=0-76. t2=75-76. |
| T0,d | Track zero sensor alignment test on drive d. t1=1-2 lp. t2=0-1 lp. t3=0-2 lp. |
| SK,d,s | Head skew test on drive d. s is optional side select (0 or 1). t1=1-76 lp. |
| RS,d,hhhh | Read sector hhhh from drive d to buffer |
| WS,d,hhhh | Write buffer to sector hhhh on drive d |
| DB | Display buffer in hex and ascii |
| FB,hhhh | Fill buffer with repeating pattern hhhh |

The running test may be aborted by escape key

The next test of the sequence is entered by depressing spa
key

Tests followed by letters "lp" move head between tracks show

Some tests require the appropriate alignment diskette and a
that it be inserted. Other tests require a scratch discette a
ask that it be inserted.

Typing OS<CR> will return the user to the operating syst
(reboot).

# FAIRLIGHT

# COMPUTER MUSICAL INSTRUMENT

# MUSIC KEYBOARDS SERVICE MANUAL

Revision 1.0

July 1982

CMI MUSIC KEYBOARDS
SERVICE MANUAL
REVISION 1.0

Fairlight Instruments Pty Ltd

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## 1. Introduction

The CMI has provision for one Master keyboard and optionally, a Slave keyboard which operates in parallel with the Master. The CMI mainframe has only one keyboard input port, to which is connected the Master keyboard. The Slave keyboard, Alpha-numeric keyboard, and other attachments such as pedal controls, all connect to the Master keyboard. The latter contains an intelligent communications interface which monitors all attached devices and routes information from them through the single channel to the CMI.

In addition to the piano type music keyboard, the Master keyboard provides three slider pot analogue controls and two switch controls (one momentary on, the other on/off) with lamp indicators whose purpose may be defined by the user by means of the CMI system software. A 12 character LED alpha-numeric display and 16 switch keypad constitutes a simple user interface to the mainframe so that during a live performance operations such as loading voices may be performed directly from the Master keyboard.

The Slave keyboard serves only as an extra music keyboard and contains none of the extra facilities of the Master keyboard.

Related Documents: The following drawings are either referred to directly in this manual or will be of use in servicing the CMI music keyboards -

| | |
|---|---|
| Exploded diagrams | DMC004 Master Keyboard |
| | DMC004B Master Keyboard with cover |
| | DMC015 Keyboard switches subassembly |
| | DMC005 Slave Keyboard |
| Drawing | DMC004C Bottom panel screw positions |
| Schematic Diagrams | MC004-01 Master keyboard wiring |
| | CMI10-00 Master controller |
| | to CMI10-02 |
| | CMI11-01 Switch module |
| | CMI12-01 Display/Keypad |
| | CMI14 Slave keyboard interface. |

## 1.1 Operating Principles

Control over all keyboard functions is centralised upon the CMI-10 Keyboard Controller which is located within the Master Keyboard. Keyboard scanning, of both master and slave keyboards, is accomplished by analogue multiplexing of the voltages on all key switches. The key switch mechanism consists of two brass buss bars running the full length of the keyboard which are supplied with +5 and -5 volts, and a delicate spring contact on each key which is allowed to move between the two buss bars as the key is pressed. By measuring the time it takes the spring contact voltage to change from -5V to +5V, the velocity with which a key is pressed may be calculated.

The analogue multiplexing is performed by the CMI-11 switch modules, each of which has provision for 24 or 25 spring contacts. Each module provides one analogue output which is the state of the contact currently addressed by the select lines from the controller, and each keyboard contains three modules. Six analogue comparators (three for the master and three for the slave) on the master controller receive these analogue signals and determine the state of the currently addressed key.

The user keypad and off/on switches are scanned in the same way although the multiplexed states are read directly as a digital signal.

The wipers of the three slider controls on the master keyboard and three plug-in pedal pots are similarly multiplexed and fed to a single analogue to digital converter on the master keyboard controller. A change detected in any analogue level read by this converter is reported to the CMI provided that change is greater than a certain tolerance set by a 6-pole DIL switch.

All information reflecting the state of the master and slave keyboards, and attached pedal controls plus characters received from the alpha-numeric keyboard are sent to the CMI through a single serial communications channel. User information received from the CMI through the same link is displayed on the LED display. The display modules accept ASCII characters directly from the keyboard controller.

At this point the three CMI-11 switch modules may be viewed with the spring switch contacts gently stretched across the brass -5V buss bar and engaged in the plastic "keyhole grips" extending from underneath each key. Each grip has two keyholes: the spring contact should always be engaged with the lower one (closest to the underside of the key).

### 2.1.4 Removal of CMI-11 switch modules (Refer to drawing DMC-015)

The following steps should be followed for each module to be removed:

(12) Remove the 10 way cable plug from its socket.
CAUTION: This cable should never be plugged or unplugged with the keyboard power applied or damage will result to the switch module circuitry.

(13) Using tweezers or fine pliers, gently grip each spring switch contact and stretch it just enough to release it from its keyhole catch. Tuck it down underneath the lower brass buss supply bar (-5V).

(14) Use a 6BA nut driver to remove the 9 nuts and star washers securing the switch module to the underside of the key assembly.

(15) Unscrew the 3 screws which pass through the buss bar support blocks to the underside of the key assembly.

(16) Lift the module off its supports.

### 2.1.5 Removal of Control Panel and Display/Keypad (Refer to drawing DMC-004)

(17) Slide the keyboard forward again as in step 10, and remove the four screws numbered 31 and 32 on the left in drawing DMC004 for the control panel, and/or the corresponding screws on the right for the display/keypad.

(18) Lower the keyboard and remove the 20 way flat cable from the display/keypad or release from its cable clips the 10 way ribbon cable leading from the CMI-10 module to the control panel. This cable is attached to the control panel.

(19) Lift the desired assembly out.

## 2.2 Master Keyboard Reassembly

Reassembly of the Master keyboard is essentially a matter of reversing the procedures of Section 2.1. Care should be exercised while replacing the CMI-11 switch modules not to damage the delicate spring switch contacts. Tighten the nine nuts and three buss bar support screws evenly to ensure the module is not warped or distorted in any way and that the buss bars are not bent.

caused by a mechanical problem in the spring switch contact mechanism. Remove the cover of the keyboard according to section 2.1.1 and hinge the key assembly up as described in section 2.1.3.

Common causes of failure are damaged, loose or dirty spring contacts, or inadequate contact between the spring and the brass buss bars.

### 3.3 Failure of Groups of Keys (Master and Slave)

If all the 24 or 25 keys scanned by a particular switch module fail to operate then the fault lies either in that module (check the voltages on both buss bars) or in the path from it to the analog key data multiplexor in the Keyboard Controller (incuding the cable.) The source of such a fault may be isolated by swapping around the flat cable connectors to the switch modules.

Failure of certain keys belonging to each module is most likely to be caused by incorrect scanning addresses arriving at the switch module: either a cable fault or an I/O problem on the keyboard controller. In this case it is unlikely that the keypad or display will work either.

If no such module-related pattern to the faulty keys exists,then the problem is mechanical. Check that all spring contacts bend across the -5V buss bar by approx 20 degrees from the horizontal when the keys are released and across the +5V bar by the same angle (in the opposite direction) when the keys are depressed. A tension spring in the back of each key returns it to the original position when it is released.

### 3.4 Slave Keyboard Malfunctions

Failure of groups of keys or individual keys on the slave keyboard can be diagnosed following the same guidelines as for the master keyboard. However two additional possible sources of faults exist: the cable from the master keyboard to the slave, and the CMI-14 slave interface. Since the slave scan address lines are the same as the master scan address lines, faults in the slave keyboard which corrupt those lines can cause the master to malfunction. Section 7.1.1 describes the use of the 4-pole DIL switch on the CMI-14 to disable individual switch module outputs when isolating slave keyboard faults. Ensure that all switches are open to enable the full keyboard velocity sensing prior to reassembling the slave.

CAUTION: Always turn off CMI power to the master keyboard before connecting or disconnecting the external cable between the master and slave. Omission to do this will cause damage to the switch modules in the slave keyboard.

## 4. Master Keyboard Controller CMI-10

The function of the CMI-10 Master Keyboard Controller card is to execute all keyboard facilities of the CMI and communicate the status of those facilities through a single serial link to the central processor. The facilities are -

Master keyboard scanning (with CMI-11 multiplexor).
Slave keyboard scanning (with CMI-14 slave interface and CMI-11 multiplexor).
Data link to CMI for the alpha-numeric keyboard.
Master keyboard keypad
Keypad display of information from CMI
Three slider pots
Two on/off switches
Three pedal controls with switches

This section describes the operation of the CMI-10.

### 4.1 MPU, Decoding, RAM, and Restart (Refer to drawing CMI10-00)

#### 4.1.1 Microprocessor Unit

The central driver of the Keyboard Controller is the 6802 microprocessor unit (MPU) at location E567 which is activated by a 4MHz crystal. At power-up the MPU reset line is held low for approx 0.4 seconds at wnich time it is released to begin execution. It is important that this restart time is less than the CMI's Central Processor restart interval to ensure that no characters sent to the Keyboard Controller are lost. The MPU may also reset manually by depressing SW1 (nearer the heatsink). This switch is debounced through the pair of open-collector NAND gates D12.

While the restart line is held low, the MPU places FFFE (hex) on the address buss and its first operation is to fetch the restart vector from locations FFFE/F. Execution is then transferred to the initialization routines in ROM. Successful completion of this power up phase is indicated by the keyboard switch lamps switcning on for about one second, off for another second, then on again. A " - POWER ON - " message is then written to the keypad display.

A 4-pole dual-in-line (DIL) switch, SW3, is used to select the source of Non-Maskable Interrupts to the MPU. This may be either from the manual switch SW2 or a clocked timing signal. The DIL switch functions as follows:

| Switch | Effect if closed |
|---|---|
| 1 | Select BRCK signal from Baud rate gen. as timing reference. |
| 2 | Select ø2 from MPU as timing reference. |
| 3 | Select SW2 as NMI |
| 4 | Select timing rerence as NMI |

Clearly, switches 1 and 2 are mutually exclusive and must not be closed simulataneously, as are switches 3 and 4. Before feeding to switch 4, the nigh frequency reference selected by switches 1 or 2 is divided by 512, 1024, 2048 or 4096 by the binary counter C5. This division ratio is determined by the p.c.b. link next to C5 (normally 2048). The divided reference (signal SCND) is used as a control line signal to the PIAs, in addition to optioning as an NMI source.

With "KBDIOA" and "VELKEYD" ROMs, switches 2 and 3 only should be closed. This selects SW2 as NMI source, and has the same effect as restart SW1 except that NMI vector FFFC/D is used. Switch 1 of the DIL switch is nearest the edge of the p.c.b. with the heatsink.

The 6802 MPU contains 128 bytes of internal RAM. This is permanently enabled by tying the Ram Enable signal (pin 36) high.

4.1.2 Address Decoding

Selection of all ROMS, external RAM and peripheral devices is performed by four LS139 1-of-4 decoders in ICs E12 and E34. Addresses are decoded when both the ø2 and VMA (Valid Memory Address) signals from the MPU are high.

The address map of the Keyboard Controller is as follows:

| Address (Hex) | Function |
|---|---|
| 0 - 7F | Internal RAM. 23 bytes only used, for software variable storage. |
| 80 - 83 | Active key input/AD conv. input PIA (K34) |
| 90 - 93 | Key address output PIA (F34) |
| A0 - A1 | Alpha-numeric keyboard comms. ACIA (C67) |
| B0 - B1 | CMI communications ACIA (D67) |
| C0 | Software readable switch |
| 4000 - 43FF | External RAM #1 (L67, N67) |
| 5000 - 53FF | External RAM #2 (K67, M67, not normally installed) |
| 9000 - 9400 | ROM #1 (J67, not normally installed) |
| A000 - A400 | ROM #2 (HI67, not normally installed) |
| B000 - B400 | ROM #3 (G67, "VELKEYD") |
| FC00 - FFFF | ROM #4 (F67, "KBDIOA") |

4.1.3 Software Readable Switch

The six-pole dual-in-line (DIL) switch SW4 provides adjustment to the sensitivity of the analogue controls. It is read whenever an A/D conversion detects a changed analogue level. Bits 4 and 5 (switches 1 and 2, nearest the heatsink) are ignored and the 4-bit number remaining gives the minimum change in the converted level required before the change will be reported to the CMI.

The switch is read through buffer N8 whose inputs are pulled high, unless grounded by a closed switch. Thus a binary '1' corresponds to an open switch.

Normally, sensitivity is set to 3 digital levels so switches 3 and 4 only are closed.

### 4.1.4 External RAM

Provision is made on the CMI-10 p.c.b. for 2K of static RAM but normally only 1K is installed: 2114s L67 and N67. Each chip contains 1K x 4 bits storage. The upper nybble is stored in L67, and the lower nybble in N67.

## 4.2 ROMs and Peripherals
(Refer to Drawing CMI10-01)

### 4.2.1 ROMs

Provision is made on the CMI-10 printed circuit board for four 2708 ROMs. Normally only two of these are installed: "KBDIOA" at location F67, and "VELKEYD" at G67. The first ROM contains the initialization and I/O firmware for the Keyboard Controller and the second contains firmware responsible for scanning the velocity sensitive keyboard and analogue and switch controls.

### 4.2.2 Serial Communications ACIAs

Serial communication with the Alpha-numeric keyboard is accomplished through the 6850 Asynchronous Communications Interface Adaptor (ACIA) at C67, while communication with the CMI utilises the 6850 ACIA at D67. The Baud rate for both ACIAs is derived from the Baud rate generator at B12 driven by a 1.8432 MHz crystal and a p.c.b. link at C12 normally selects 9600 Baud operation (pin 1 of B12).

The Baud rate generator also provides the BRCK signal, normally linked to 1200 Baud at B45.

Both ACIAs are normally linked via LK1 and LK2 to the common interrupt request (IRQ) buss signal. D67 generates IRQs when transmitting to and receiving from the CMI, while C67 generates IRQs when receiving from the Alpha-numeric keyboard.

### 4.2.3 Peripheral Interface Adapters (PIAs)

Two PIAs are used, each containing two 8-bit parallel I/O ports and four control outputs/IRQ input lines. The PIAs are configured during initialization and used as follows:

PIA F34

| | |
|---|---|
| I/O port A<br>PA0 - PA1 | Peripheral address outputs. Buffered through G23 to address to provide:<br>CMI-11 switch module addresses<br>CMI-12 keypad mutiplexor addresses<br>LED display module data<br>Data inputs to flip-flops (G4) which switch control button lamps.<br>Analog control input multiplexor addresses. |
| CA1 | Scan Not Done (SCND) timing flag input |
| CA2 | Strobe output to update lamp flip-flops |
| I/O port B<br>PB0 - PB1<br>PB2 - PB7 | LED display digit select lines<br>LED display all-segments-on (CU) and module select (CS) signals. |
| CB1 | Input flag from keypad multiplexor. Does not generate IRQs. |
| CB2 | Strobe output to update a LED display ($\overline{DWS}$) |

PIA K34

| | |
|---|---|
| I/O port A<br>PA0 - PA5 | Inputs from music key threshold comparators |
| PA6 | Input from control switch multiplexor enabled by BKA7 |
| PA7 | Input from keypad multiplexor, also enabled by BKA7 |
| CA1 | Inverted timing reference input. Does not generate IRQs. |
| CA2 | Threshold select output |
| I/O port B<br>PB0 - PB7 | Data inputs from A/D converter (ADC) |
| CB1 | $\overline{DR}$ (Data Ready) flag from ADC |
| CB2 | B/$\overline{C}$ (Begin Conversion) strobe to ADC |

## 4.3 Power Supplies and Analog Interface Section (Refer to drawing CMI-10-02)

### 4.3.1 Power Supplies

The Keyboard Controller receives +20V, -20V and +10V from the CMI through a 6-pin Utilux connector. Six on-board regulators are used to generate three independant +5V supplies, in addition to +12V, -12V and -5V supplies. These power the Controller itself plus the keypad display, slider and pedal pots and switches.

The supply designated "+5V" powers all circuitry on drawings CMI-10-00 and CMI10-10-01 except the ROMs, which are powered separately from "+RV". The analog multiplexors, A/D converter and RS-232 drivers on CMI-10-02 recieve power from "+XV" and where necessary, the -5V supply.

"+XV" also leaves the Controller board to power the CMI-11 keyboard switch multiplexors, and the keypad display.

### 4.3.2 Threshold Detection

MD1-3 and SD1-3 are the multiplexed signals representing the position of music keys addressed by the three master keyboard CMI-11 modules and the slave keyboard interface CMI-14, respectively. These signals are compared by the six MLM311s to a known threshold to determine when a key begins to be pressed, and when it is fully depressed.

The THLD signal from PIA K34 sets up one of two thresholds through the 741SC level shifter. If THLD is low, a -2.7V threshold is applied to the comparators. With THLD high, the threshold is +2.3V.

Initially, THLD is low. An unpressed key rests against the -5V buss bar so the corresponding comparator output will be high.When the key is first depressed and the spring contact leaves the -5V buss bar, the output of the module<when that key is selected is pulled to just below zero volts by a 10k resistor to ground on the switch module and a 100k resistor to -5V on each comparator input. This causes the comparator to change state to a low. The change is read from the PIA whereupon THLD is switched high to select the +2.3V threshold, setting the comparator high again. It will return low when the key reaches the +5V buss bar at its full depression. The time taken between the two falling edges of the comparator output is noted by the MPU, and this mechanism forms the basis of the velocity sensitive keyboard.

The key continues to be compared to the +2.3V threshold until its release is detected.

### 4.3.3 Control Signal Multiplexors and A/D Convertor

User control signals enter the Keyboard Controller from several possible sources: two control panel sw<tches, three pedal switches, three control panel slider pots and three pedal pots. The switch controls are analogue multiplexed by H3 and read directly as KD6 when gated by a high level on BKA7.

The analogue controls (slider and pedal pots) are multiplexed by I3, buffered by 741SC I4, and fed to the AD570 A/D converter at J4. The low frequency signals used do not require a sample and hold. The converter is strobed to begin a conversion by the B/$\overline{C}$ signal from the CB2 output of PIA K34 and flags the end of conversion to CB1 of the same PIA.

The sensitivity of the analogue controls may be set by DIL switch SW4. Refer to section 4.1.3 for further details.

### 4.3.4 RS-232 Interface

ICs A5 and A6 are the RS-232 drivers for the two ACIAs described in section 4.2.2 .

### 4.3.5 Lamp driver

The control panel lamps are supplied with 20V and switched on when the MC75452 driver at J2 pulls the appropriate line to ground. The driver is activated by signals LP1 and LP2 latched from PIA F34.

### 4.3.6 Connections

The Keyboard Controller requires four external connections as follows:

SO1 50 Way flat cable connector.

| | |
|---|---|
| Pins 1-5 | Master switch module 1 scan address |
| 6 | N/C |
| 7 | -5V to Master switch module 1 |
| 8 | "+XV" 5V to module 1 |
| 9 | Ground to module 1 |
| 10 | MD1 module 1 multiplexed output |
| 11-20 | Master switch module 2 connections as for 1 |
| 21-30 | Master switch module 3 connections as for 1 |
| 31-37 | Scan address to keypad and data lines to LED display |
| 38 | All segments on, display module 0 (CU) |
| 39 | Module select, module 0 (CS) |
| 40-41 | CU and CS lines, display module 1 |
| 42-43 | CU and CS lines, display module 2 |
| 44-45 | LED display digit select |
| 46 | Digit write strobe |
| 47 | Keypad multiplexed output |
| 48 | $\overline{BKA3}$, selects keypad multiplexor 2 |
| 49 | Ground to display/keypad |
| 50 | "+XV" +5V to display/keypad |

SO2 10 Way rainbow cable connector

| | | |
|---|---|---|
| Pins | 1-2 | Button lamps switched returns |
| | 3 | Switch 2 (momentary on) |
| | 4 | Switch 1 (push on/push off) |
| | 5 | Slider pot 3 wiper |
| | 6 | +20V to lamps |
| | 7 | -5V to pots |
| | 8 | "+XV" +5V to pots |
| | 9 | Slider pot 2 wiper |
| | 10 | Slider pot 1 wiper |

SO3 26 Way rainbow cable connector

| | | |
|---|---|---|
| Pins | 1 | Pedal 1 pot wiper |
| | 2 | Pedal 1 switch |
| | 3 | Pedal 2 pot wiper |
| | 4 | Pedal 2 switch |
| | 5 | Pedal 3 pot wiper |
| | 6 | Pedal 3 switch |
| | 7-11 | Slave keyboard scan address |
| | 12 | Slave keyboard ground |
| | 13-15 | Slave switch module outputs |
| | 16 | RTS flag to alpha-numeric keyboard |
| | 17 | CTS flag to A/N keyboard |
| | 18 | A/N keyboard ground |
| | 19 | Data to A/N keyboard |
| | 20 | Data from A/N keyboard |
| | 21 | Ground |
| | 22 | CTS flag from CMI |
| | 23 | RTS flag to CMI |
| | 24 | Ground |
| | 25 | Data from CMI |
| | 26 | Data to CMI |

SO4 6 Way Utilux Connector

| | | |
|---|---|---|
| Pin | 1 | +10V return |
| | 2 | +10V |
| | 3 | +20V |
| | 4 | -20V |
| | 5 | Ground |
| | 6 | +/-20V return |

## 4.4 Software Loop and Interrupt Routine

A useful clue wnen fault finding ROM-based equipment such as the CMI-10 is the main software loop which the processor normally executes in the "steady state": that state which exists after a successful power-on initialisation, but before any special functions have been called upon by key presses, changed A/D values, etc. This software loop may also be referred to as the "idle loop". Knowledge of what happens in the idle loop allows a service person to establish, for example, what peripherals are not being regularly accessed as they should.

The program flow of the idle loop in "VELKEYD" is as follows:

```
begin loop

    for keyselect = 1 to 32

       read key-pressed pattern from comparators

       for module select = 1 to 6 (3 master, 3 slave)

           update statuses in RAM of keys pressed

       end for

    end for

    read one of the control functions and update status
    (slider pots, pedal pots and switches)

    scan entire keypad for a keystroke

    wait for rising edge of SCND flag

end loop
```

The key scan loop executes 32 times because there are 5 key select lines but there are only 24 or 25 keys on each module so some iterations of the inner loop do not correspond to any real key. A different control function is monitored and updated on each iteration of the main loop.

A knowledge of the sources of interrupts and the functions performed in the interrupt service routine(s) can be similarly useful when fault tracing. In the KBDIOA firmware, there are three possible sources of interrupts (IRQ's):

1. A character has been received from the CMI.
2. A character previously transmitted to the CMI has completed transmission from the ACIA.
3. A character has been received from the alpha-numeric keyboard.

Characters received from the CMI are written to the LED display immediately. A transmit-complete interrupt causes the processor to check the output character queue and send another character if it is not empty. A character received from the alpha-numeric keyboard is placed on the output character queue

unless the received character is actually a BREAK level, in which case a BREAK level is transmitted to the CMI.

The short piece of code which places characters on the output queue (and enables the transmitter interrupt) is actually a software interrupt routine, called by the SWI instruction ratner than a subroutine call.

## 5. Keyboard Switch Module CMI-11

Three Keyboard Switch Modules are installed in each master and slave keyboard used with a CMI. Each module provides a single signal out which represents the state (pressed, released, or in flight) of one of the 24 or 25 keys addressed by the multiplexor inputs. This section describes the operation of the CMI-11.

### 5.1 Keyboard Switch Module Operation (Refer to drawing CMI-11-01)

Five key address bits are provided provided by the Keyboard Controller CMI-10 as inputs to the CMI-11. The lower three of these are bussed across three 4051 analogue multiplexors (ICs 2-4) so that each 4051 selects one of eight spring key contacts as its analogue input. Normally, a key rests against a -5V buss bar, but when fully depressed, it contacts a +5V buss bar. In between, it contacts neither.

The outputs of ICs 2-4 are fed to another multiplexor, IC1, whose select inputs are the upper two bits of the key address. Thus the output of IC1 may be any of the 24 key contacts accessed by ICs 2-4. It may alternatively be the 25th key contact which is fed directly to IC1 as a fourth analogue input.

Each CMI keyboard has a total of 49 keys so the 25th key is only used on the extreme right hand switch module. Provision is made on the switch module p.c.b. for a 10k resistor (R1) pulling to ground. This is to ensure that if the 25th key is not installed, it appears to the multiplexor as a key which is never pressed. However, the resistor must be removed if the 25th key is installed or the velocity sensing mechanism will not work on that key.

The output of IC1 is fed directly to the Keyboard Controller in a master keyboard or to the Slave Interface in a slave keyboard. Its unused inputs are grounded.

### 5.2 External Connections

SO1 10 Way flat cable

| | | |
|---|---|---|
| Pins | 1-5 | Key scan address inputs |
| | 6 | N/C |
| | 7 | -5V supply |
| | 8 | +5V supply |
| | 9 | Ground |
| | 10 | Multiplexed analogue output |

## 6. Keyboard Display and Keypad Module CMI-12

Tne Display and Keypad Module provides a simple user interface with the CMI from the master music keyboard. A 16-switch keypad is scanned by the Keyboard Controller for commands to be sent to the CMI and a 12 digit LED display receives simple messages from the CMI to the user. This section describes the operation of the CMI-12.

### 6.1 Display and Keypad Operation
(Refer to drawing CMI-12-01)

#### 6.1.1 LED Display

The DL-1416 LED display modules, containing four digits each, accept 7 bit ascii codes from the data lines to display the desired character. The key scan addresses are used as data inputs. Data is latched into the modules whose chip select line ($\overline{CS}$) is low on the falling edge of $\overline{DWS}$. The DA lines select which digit within the selected module(s) is written to. The $\overline{CU}$ line is a test <nable line which causes every segment in each digit to light up.

#### 6.1.2 Keypad

The keypad is simply an array of 16 momentary switches which connect to the common (+5V) line when pressed. Two 4051 1-of-8 analogue multiplexors scan the keypad. Their select and inhibit inputs are taken from the key scan address lines. Only enabling one multiplexor at a time allows the outputs to be wired together on the same KPAD signal.

### 6.2 External Connections

SO1 20 Way Ribbon cable connector

| | |
|---|---|
| Pins 1-2 | Digit select |
| 3,5,7 | Display module select |
| 4,6,8 | Display module test (all segments on) |
| 10 | Digit write strobe |
| 9,18, 11-16 | Key scan address and data to display modules |
| 17 | Keypad multiplexed output |
| 19 | Ground |
| 20 | "+XV" +5V supply |

## 7. Slave Keyboard Interface CMI-14

The Slave Keyboard Interface provides regulated power supplies to the CMI-11 switch modules in a slave keyboard and buffers the analogue outputs of the switch modules before feeding them to the master keyboard controller. This section describes the operation of the CMI-14.

### 7.1 Operation
(Refer to drawing CMI-14)

#### 7.1.1 Scanning and Buffering

The five slave key scan address lines from the master keyboard controller are fed straight through to the CMI-11 switch modules. The output from each module is buffered by a 741SC in a non-inverting configuration and fed to the master controller. A 4-pole dual-in-line (DIL) switch allows the input of each buffer to be pulled to nearly -5V for testing purposes. In the event of a switch module being unplugged, closing the switch corresponding to that module simulates all keys released. Two or more floating buffer inputs result in the keyboard controller going into overflow due to sensing too many keys pressed. All switches should normally be open, otherwise the velocity sensing system will not work.

#### 7.1.2 Power Supplies

The CMI-14 is supplied with +20V and -20V from the CMI via the master keyboard. A 4V7 zener is used on each supply side to provide +12V and -12V to the 741 buffers, and 7805 and 7905 refulators send +5V and -5V respectively to the switch multiplexors.

### 7.2 External Connections

SO1 30 Way flat cable connector to Keyboard Switch Modules.

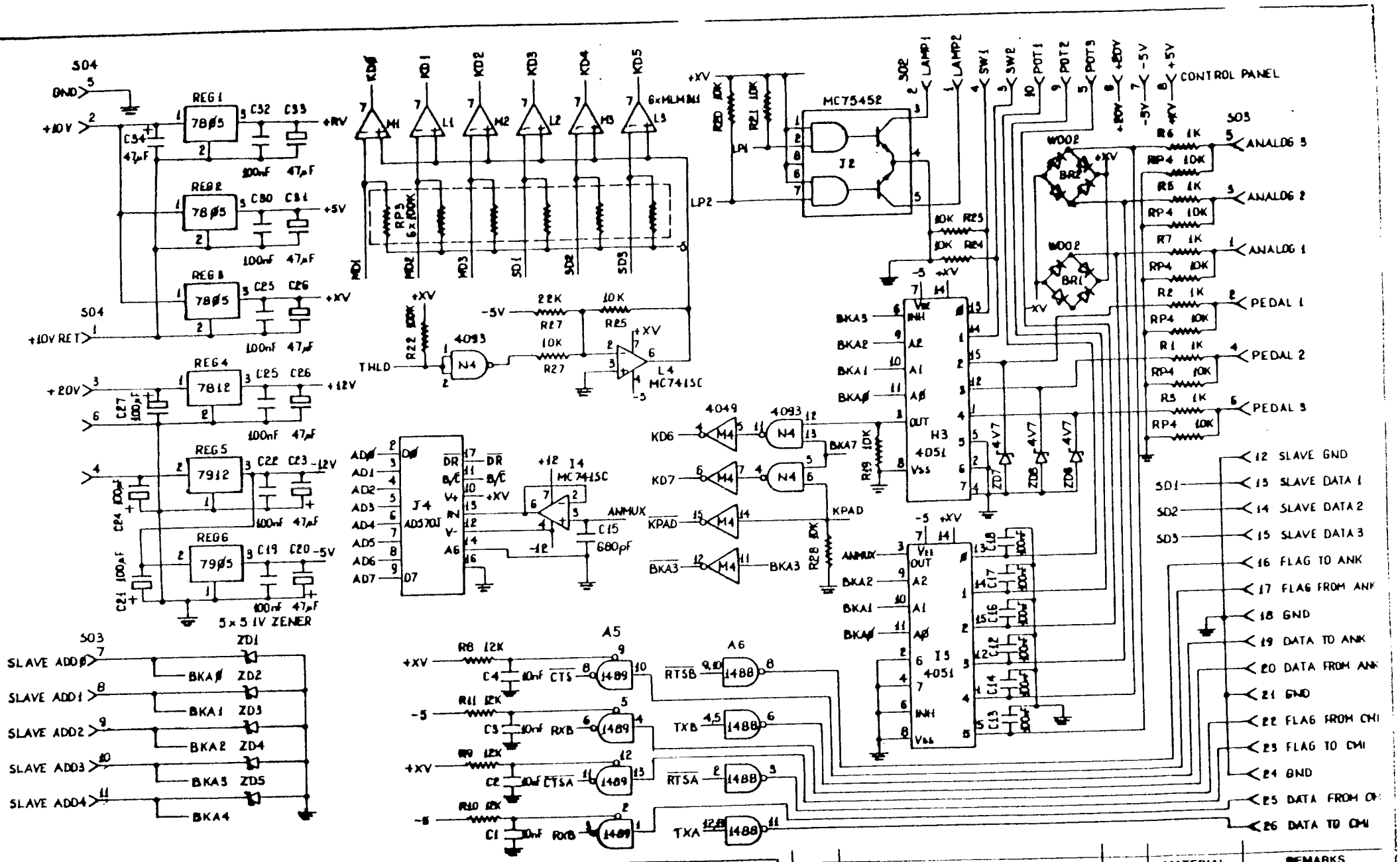
Pins 1-5 Slave switch module 1 scan address
6 N/C
7 -5V to Slave switcn module 1
8 "+XV" 5V to module 1
9 Ground to module 1
10 MD1 module 1 multiplexed output

11-20 Slave switch module 2 connections as for 1

21-30 Slave switch module 3 connections as for 1

SO2 25 Way D mini series external connector to master keyboard.

| | | |
|---|---|---|
| Pins | 1-2 | Ground |
| | 3-7 | Slave keyboard scan addresses |
| | 8 | Ground |
| | 9-11 | Slave multiplexor outputs |
| | 12-21 | N/C |
| | 22-23 | -20V supply |
| | 24-25 | +20V supply |



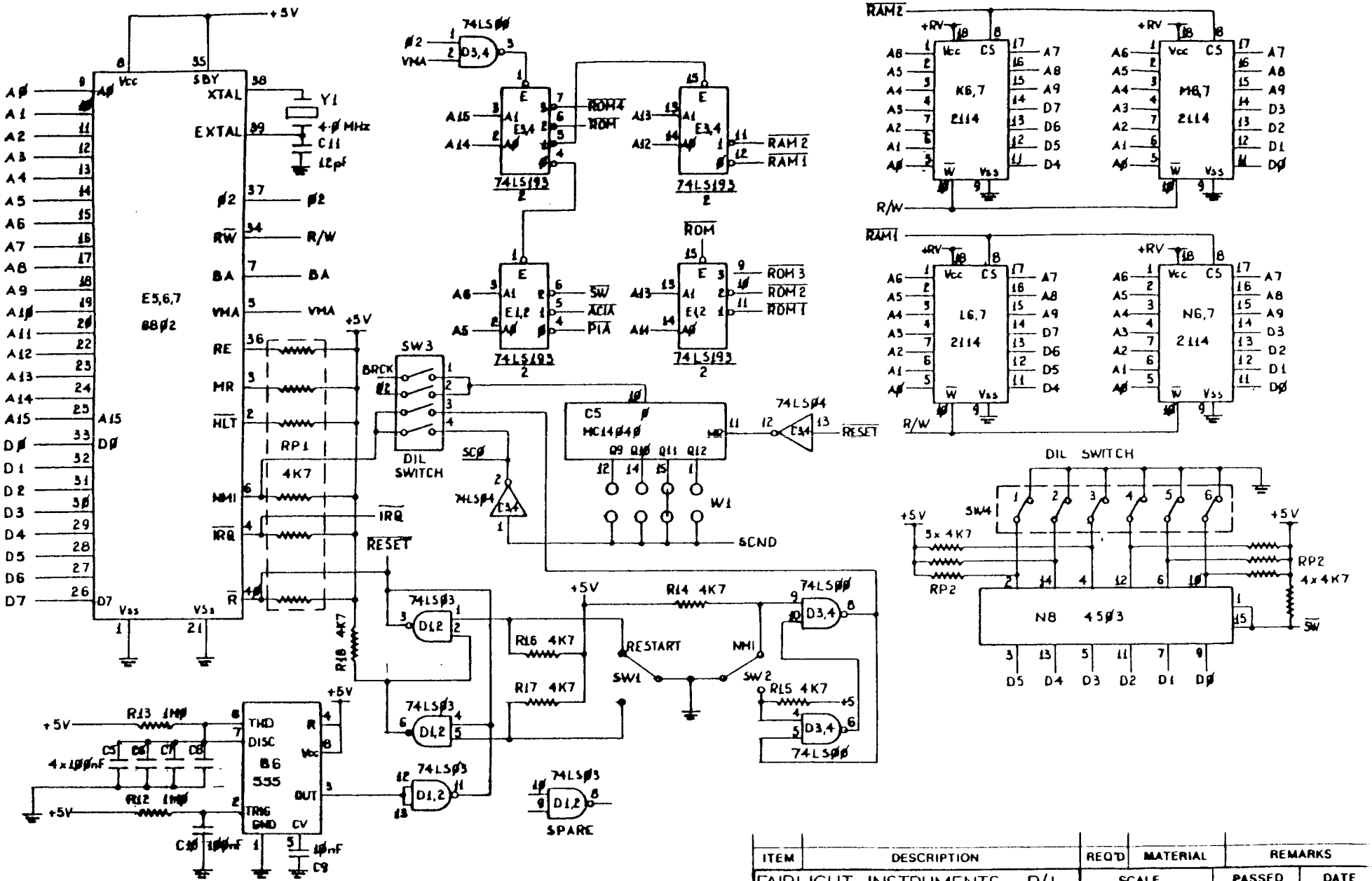

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | | SCALE | | PASSED / DATE |
| | | | | 26/6/1982 / 15/2/1980 |

FAIRLIGHT INSTRUMENTS P/L
15 BOUNDARY ST RUSHCUTTERS BAY 2011
(02) 335222

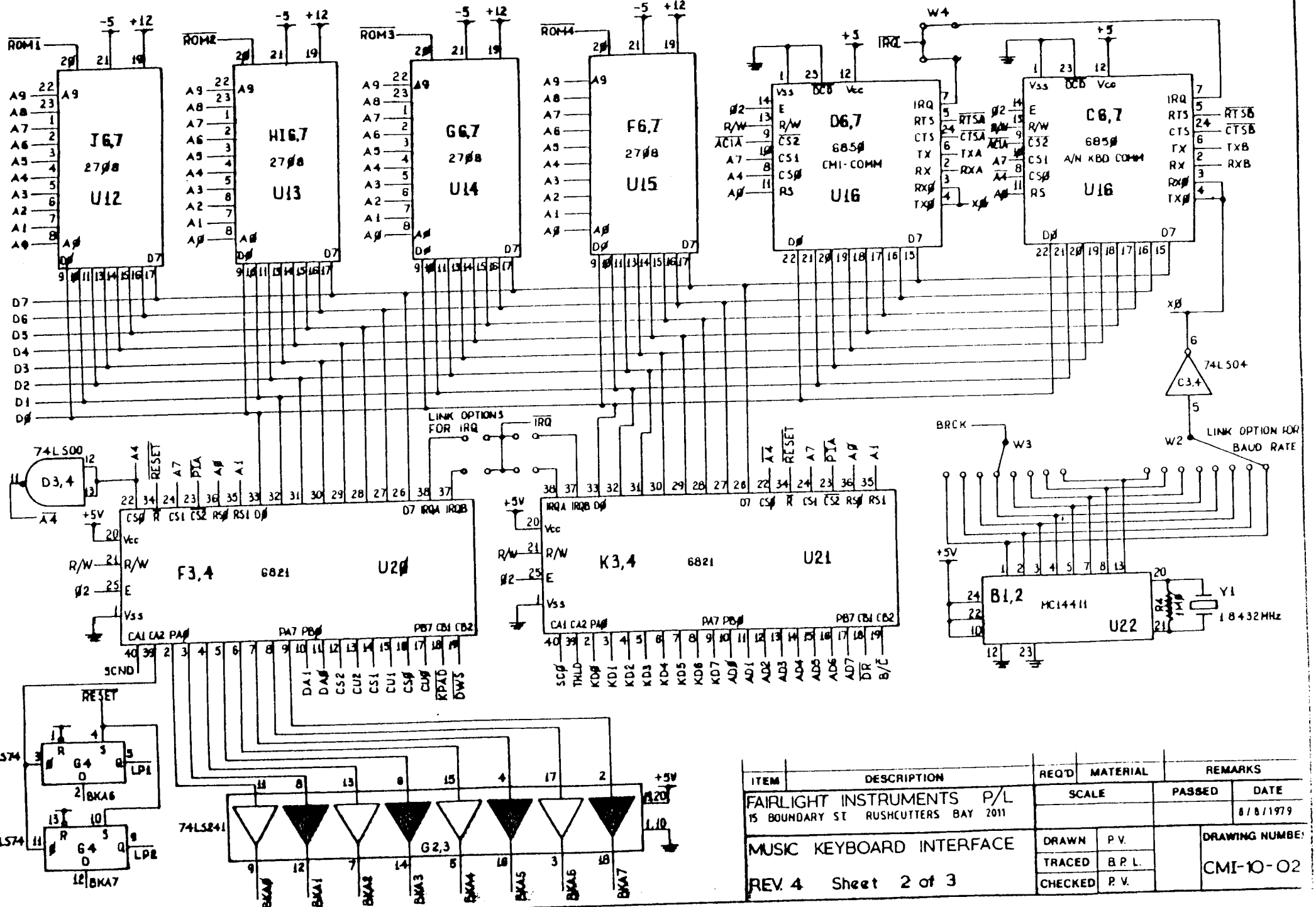
MUSIC KEYBOARD INTERFACE
REV. 4
Sheet 3 of 3

| | |
|---|---|
| DRAWN | P.V |
| TRACED | B.P.L |
| CHECKED | P.V |

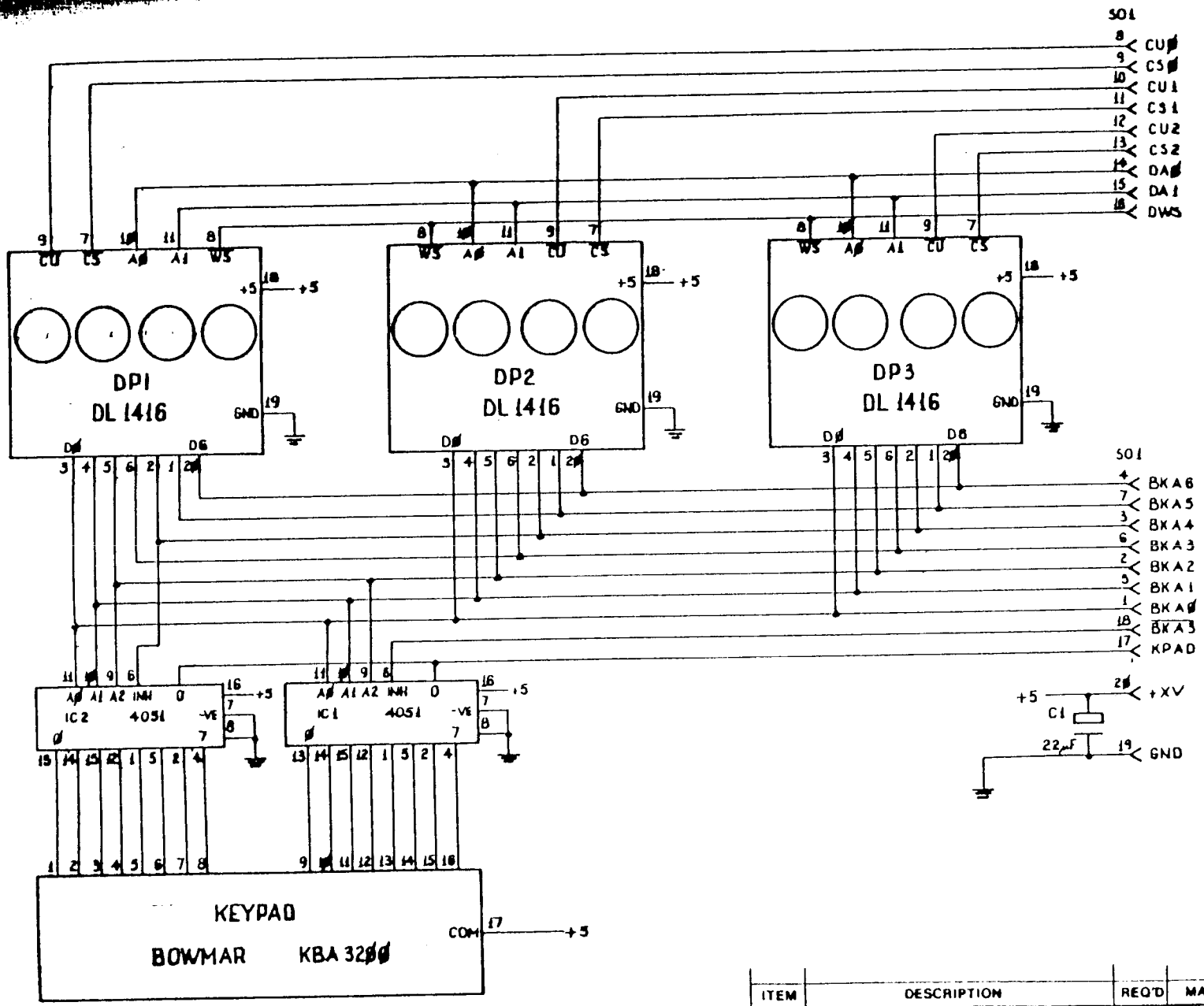
DRAWING NUMBER
CMI-10-03



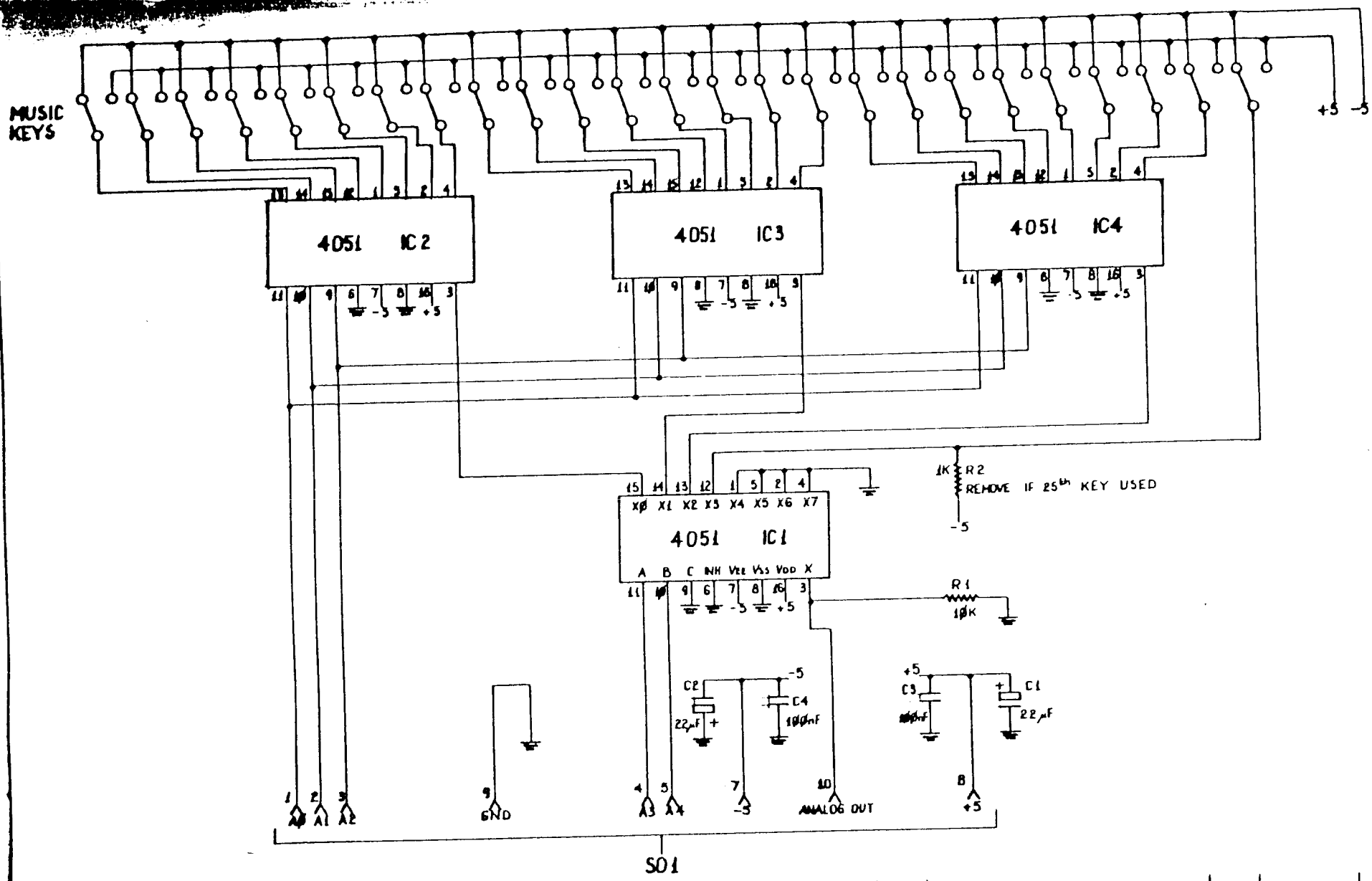

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>15 BOUNDARY ST. RUSHCUTTERS BAY 2011<br>(02) 335222 | | SCALE | PASSED | DATE |
| | | | 26/8/1982 | 6/8/1979 |
| MUSIC KEYBOARD INTERFACE<br>REV. 4 | | DRAWN P V<br>TRACED B P L. | | DRAWING NUMBE<br>CMI-10-0' |



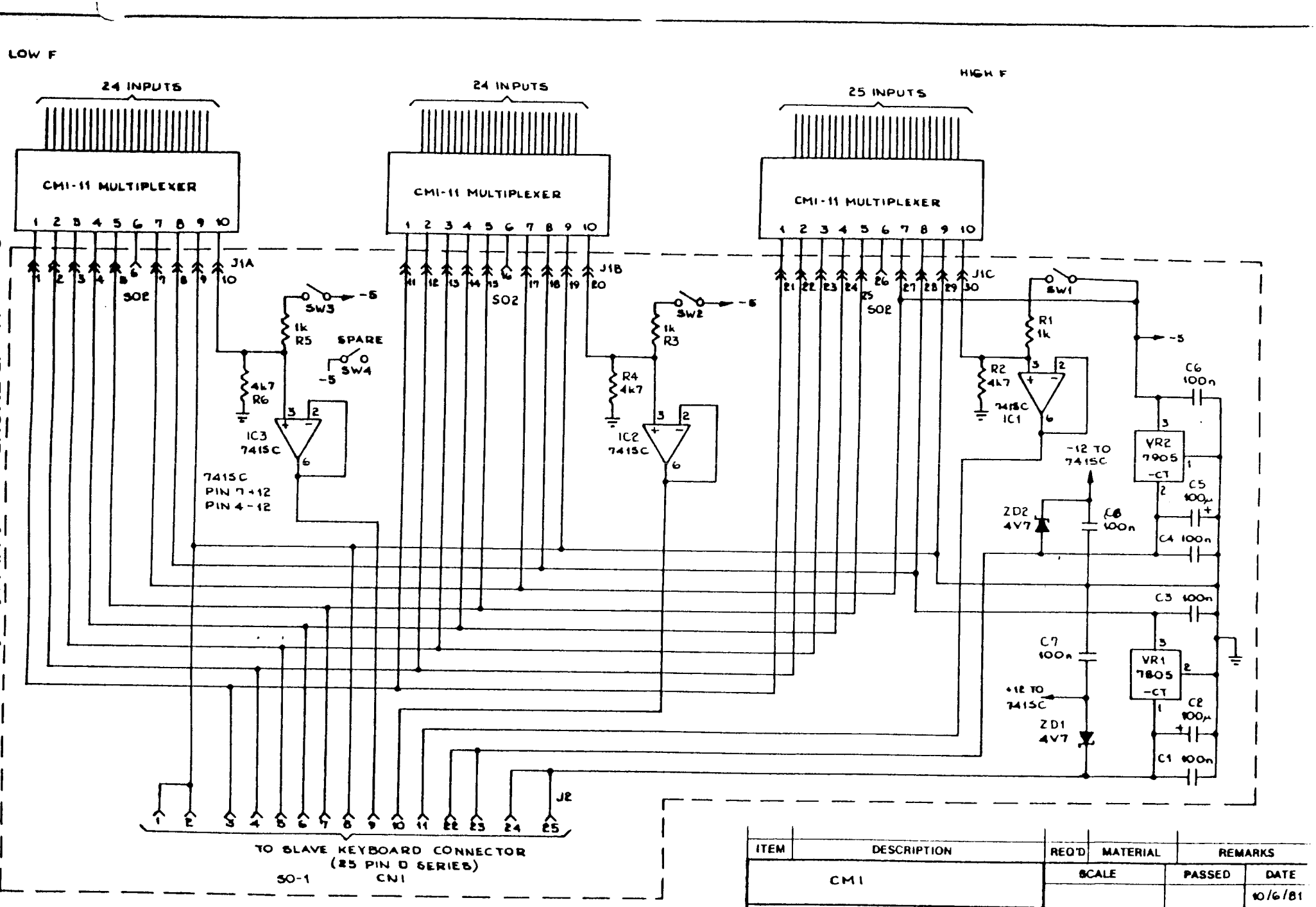

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>15 BOUNDARY ST RUSHCUTTERS BAY 2011 | | SCALE | | PASSED / DATE: 8/8/1979 |
| MUSIC KEYBOARD INTERFACE | | DRAWN: P.V. | | DRAWING NUMBER: CMI-10-02 |
| REV. 4 Sheet 2 of 3 | | TRACED: B.P.L. | | |
| | | CHECKED: P.V. | | |



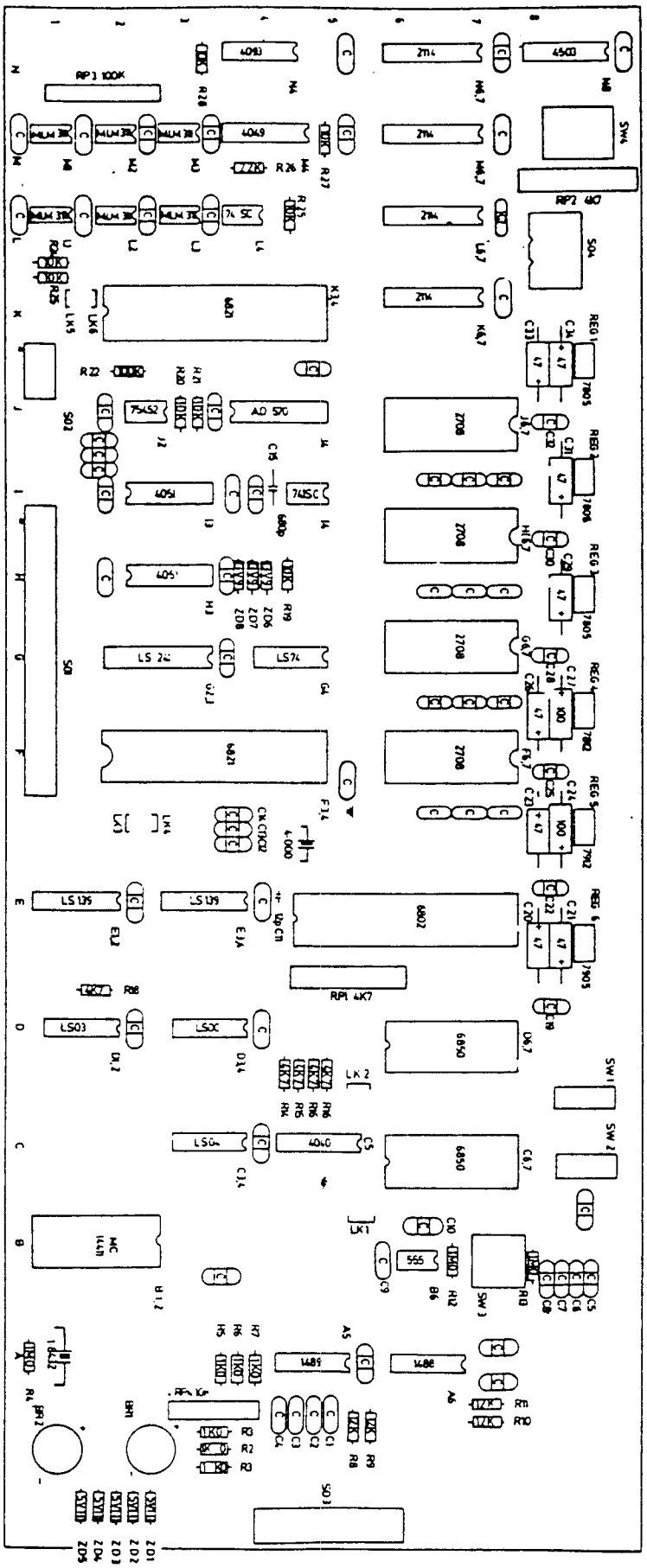

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>15 BOUNDARY ST RUSHCUTTERS BAY 2011<br>(02) 335222 | | SCALE | | PASSED 26/6/1982 DATE 10/8/1979 |
| KEYPAD / DISPLAY MODULE | | DRAWN P.V<br>TRACED B.P.L<br>CHECKED P.V. | | DRAWING NUMB<br>CM1-12-0 |
| Sheet 1 of 1 | | | | |

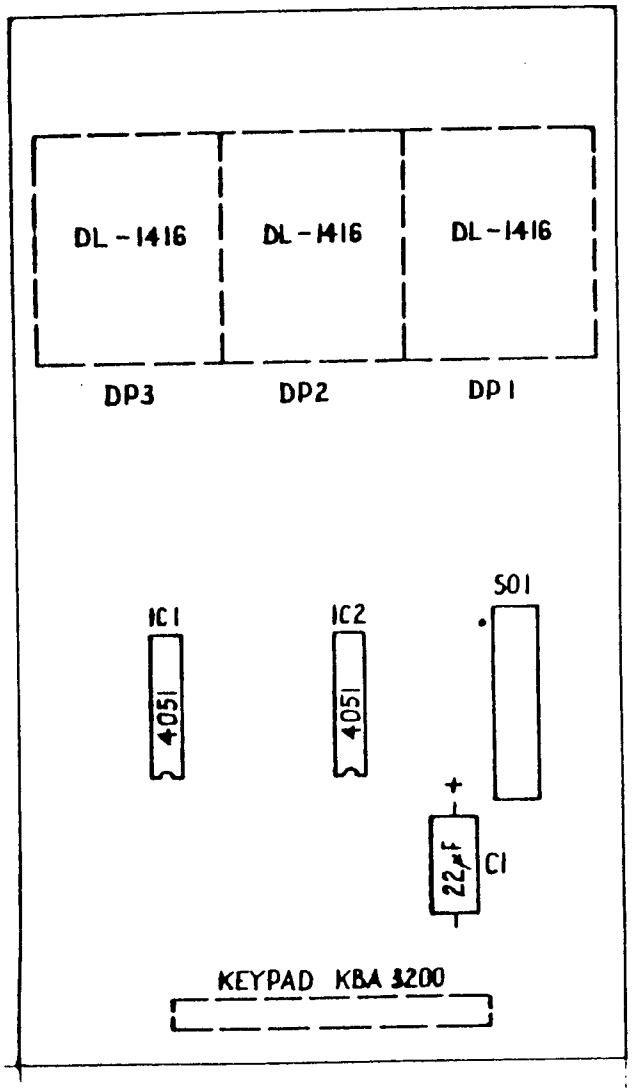



| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>15 BOUNDARY ST RUSHCUTTERS BAY 2011<br>(02) 335222 | | SCALE | | PASSED: 26/6/1982 |
| KEYBOARD SWITCH MODULE<br>REV. 3, 4<br>Sheet 1 of 1 | | DRAWN: P.V<br>TRACED: B.P.L<br>CHECKED: P.V | | DRAWING NUM: CME-11-C |

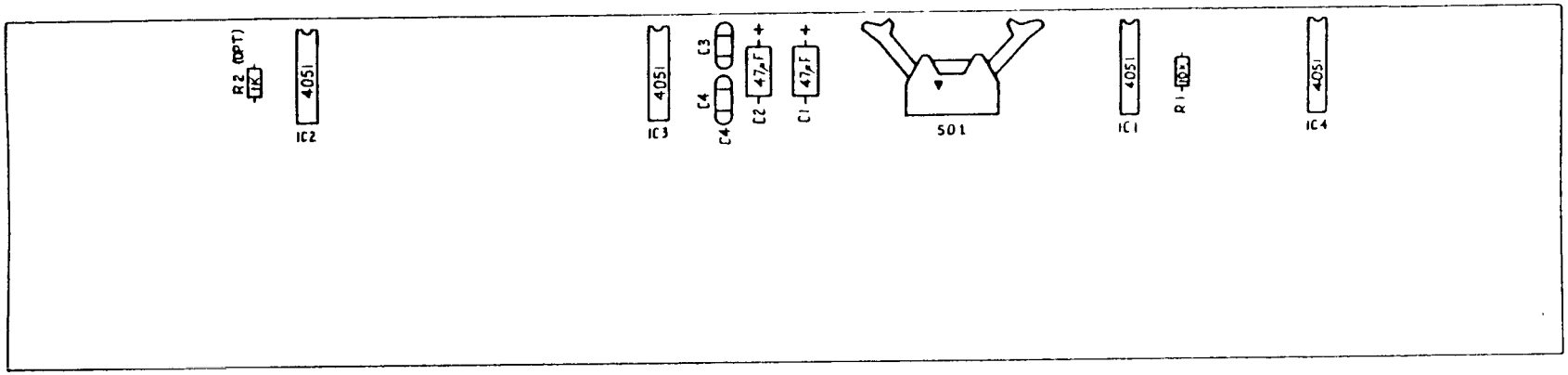



| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| CM1 | | SCALE | | PASSED / DATE: 10/6/81 |
| SLAVE INTERFACE | | DRAWN: PV | | DRAWING NUMBER: CMI-14-01 |
| | | TRACED: MTB | | |

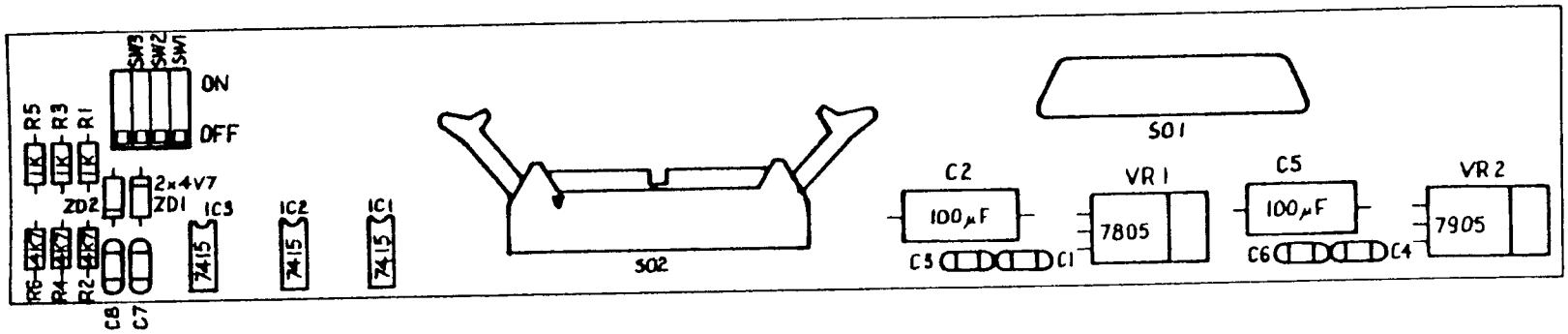





| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>15 BOUNDARY ST RUSHCUTTERS BAY 2011<br>(02) 335222 | | SCALE | | PASSED / DATE<br>15/6/ |
| OVERLAY FOR CMI-12<br>REV. 1 | | DRAWN B.G<br>TRACED B.P.L.<br>CHECKED P.V. | | DRAWING NO<br>CMI-12-C |




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>35 BOUNDARY ST RUSHCUTTERS BAY 2011<br>(02) 331 5222 | | SCALE | | PASSED |
| OVERLAY FOR CMI-11<br>REV 4 | | DRAWN | D G | DRAWING<br>CMI-11 |
| | | TRACED | B P L | |
| | | CHECKED | P V | |




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| FAIRLIGHT INSRUMENTS P/L<br>15 BOUNDARY ST RUSHCUTTERS BAY 2011<br>(02) 335222 | | SCALE | | PASSED / DATE |
| OVERLAY FOR CMI-14<br>REV 2 | | DRAWN | | DRAWING NUM. |
| | | TRACED | B P L | CMI-14-C |
| | | CHECKED | | |

CMI 14

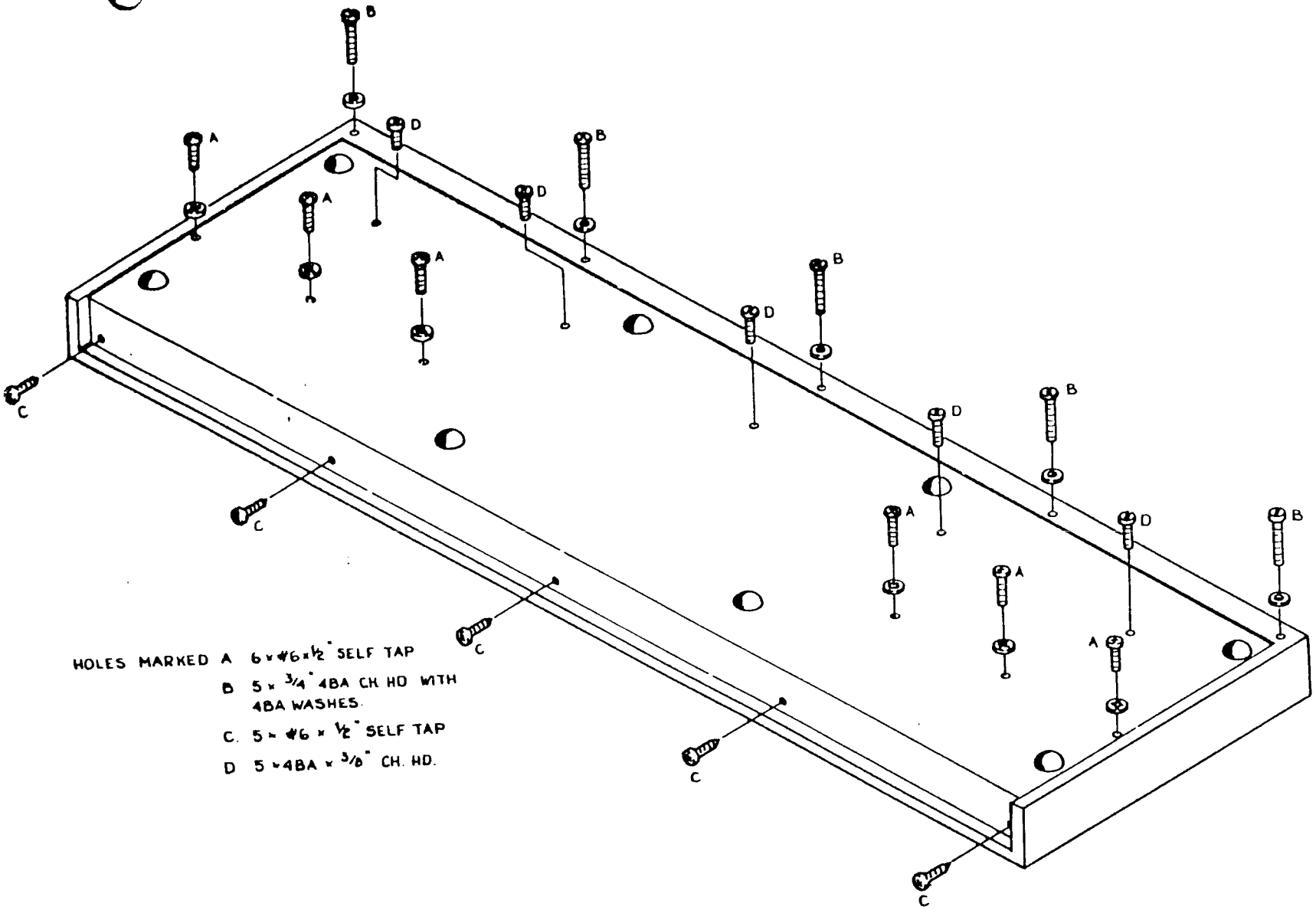
SLAVE K/BD INTERFACE CARD

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| IC1-3 | 741SC | OP AMP |
| ZD1,2 | 4V7 | |
| SO1 | 25 WAY | D TYPE |

| LOC. | TYPE | DESCRIPTION |
|---|---|---|
| REG1 | 7805 | 5V |
| REG2 | 7905 | -5V |
| SO2 | 30 WAY | HEADER |

| | RESISTORS |
|---|---|
| R1 | 1K |
| R2 | 4K7 |
| R3 | 1K |
| R4 | 4K7 |
| R5 | 1K |
| R6 | 4K7 |

| | CAPACITORS |
|---|---|
| C1 | 100N |
| C2 | 100UF |
| C3,4 | 100N |
| C5 | 100UF |
| C6-8 | 100N |



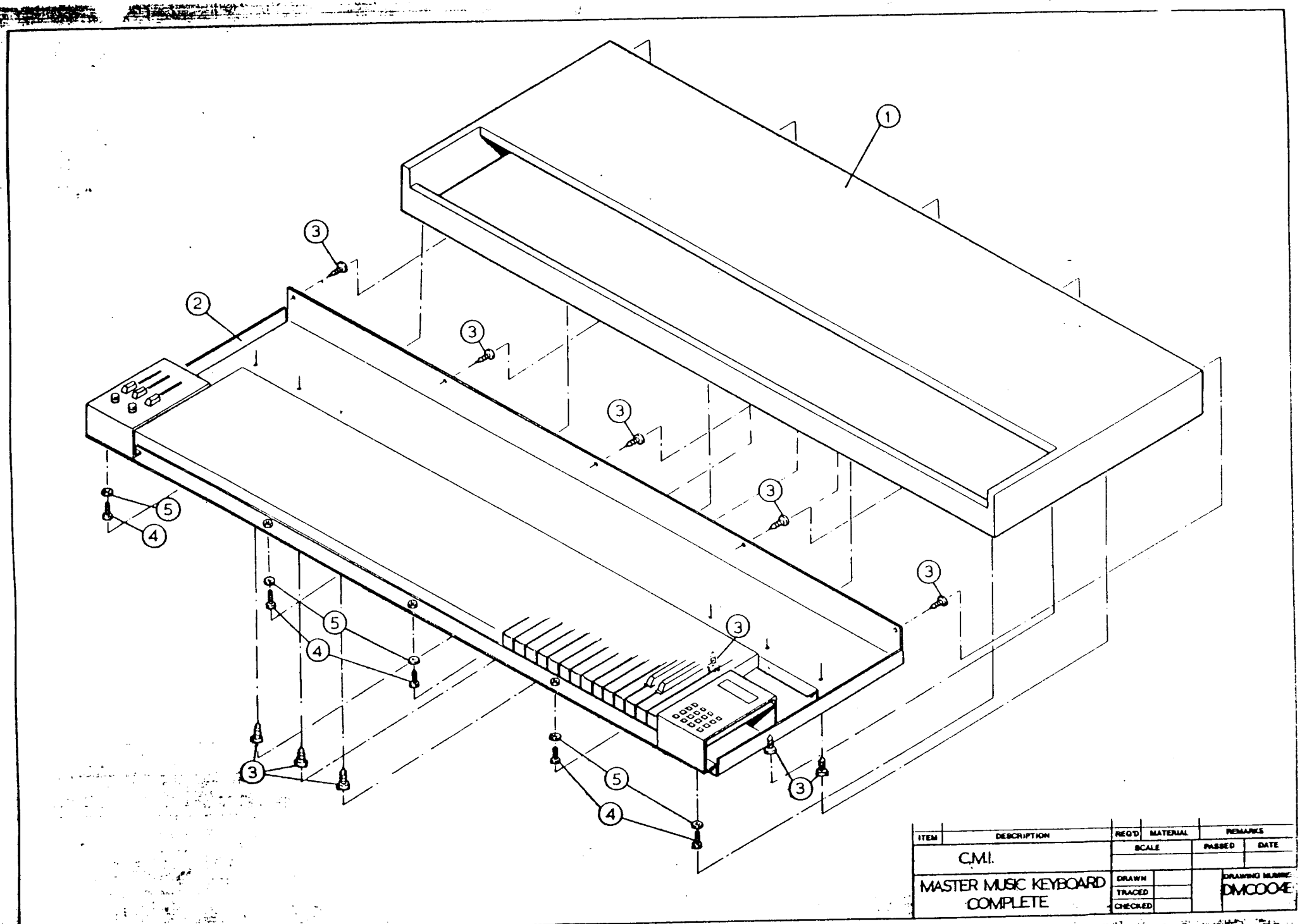

HOLES MARKED A 6 × #6 × ½" SELF TAP

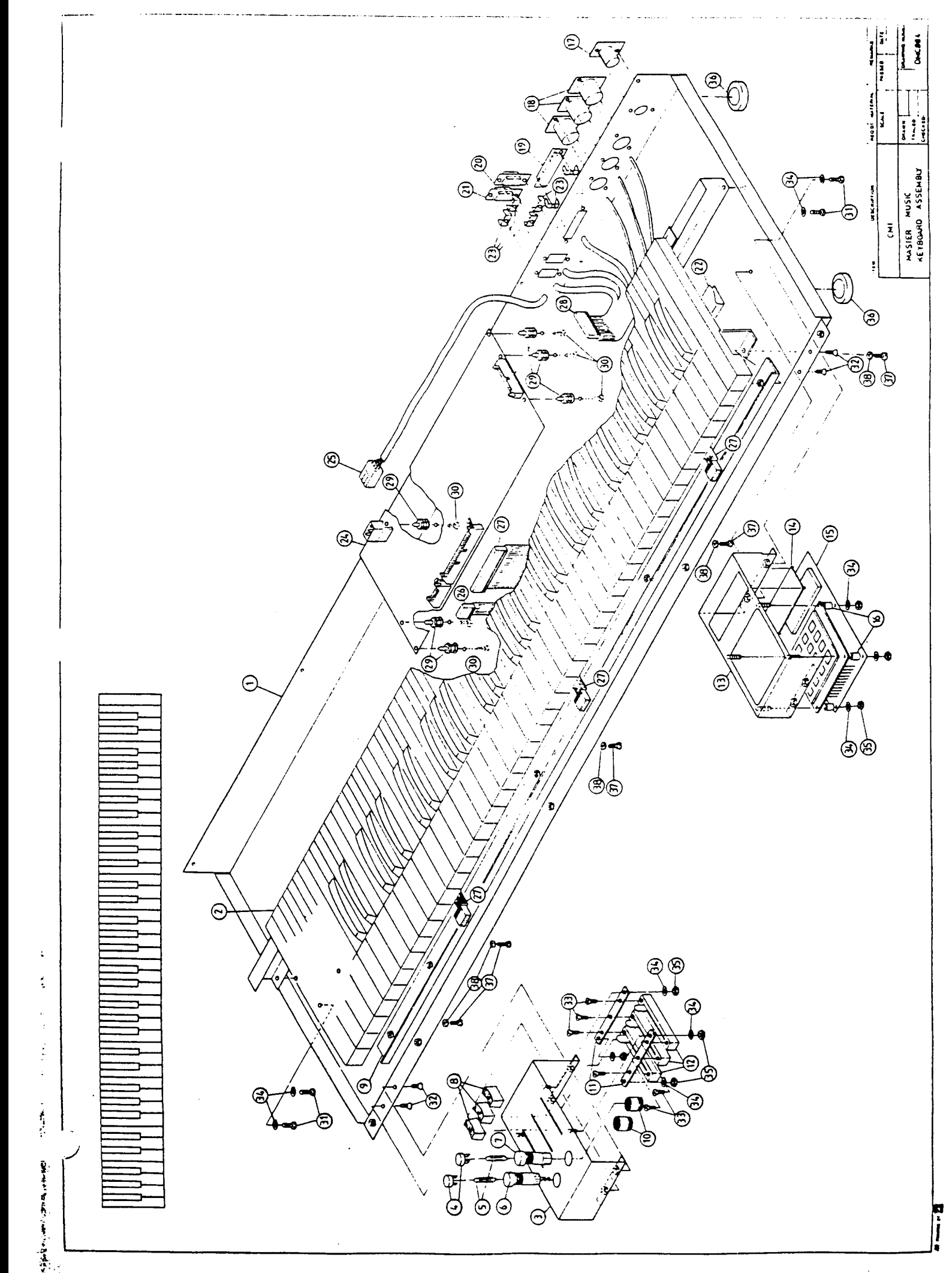
B 5 × ¾" 4BA CH HD WITH 4BA WASHES

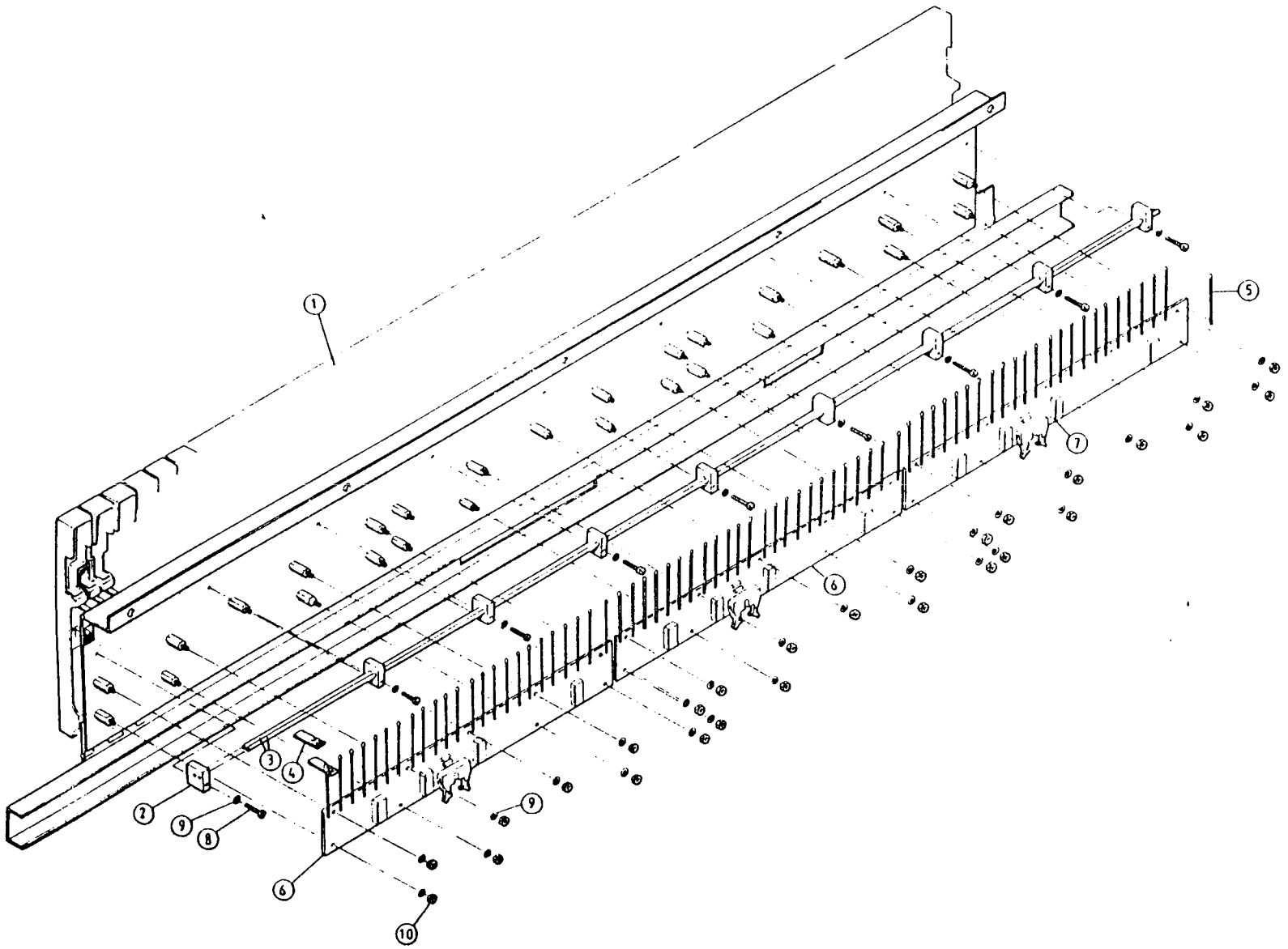
C. 5 × #6 × ½" SELF TAP

D 5 × 4BA × ⅜" CH. HD.

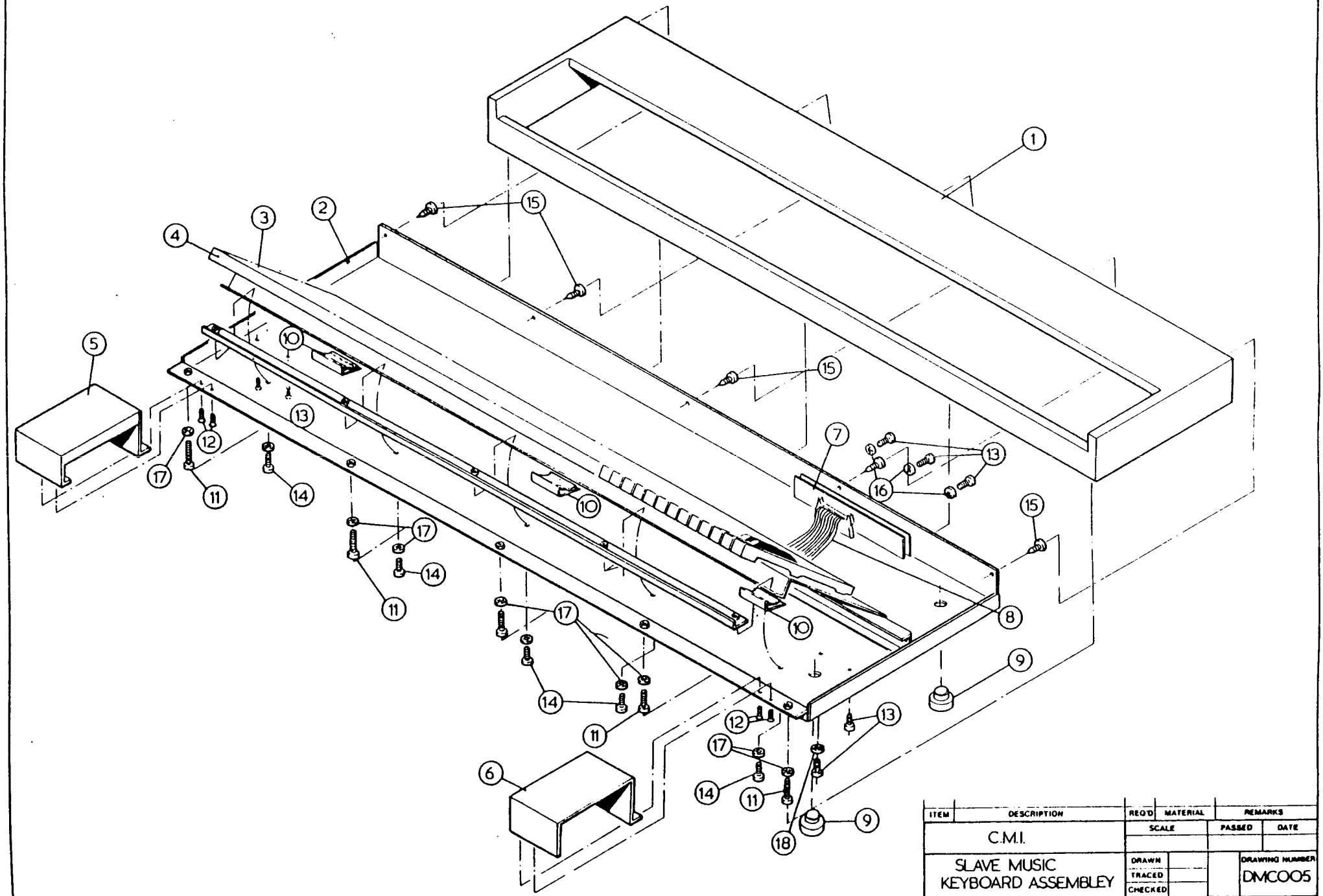
| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | C.M.I. | SCALE | | PASSED / DATE: 5/12/80 |
| | EXPLODED VIEW OF FIXING SCREWS ON MASTER KEYBOARD TOP COVER | DRAWN: MTB; TRACED; CHECKED: C.T. | | DRAWING NUMBER: DMC004C |








| ITEM | DESCRIPTION | REQD | MATERIAL | REMARKS |
|---|---|---|---|---|
| | CMI | SCALE | PROMO | DATE |
| | MUSIC KEYBOARD SUBASSEMBLY | DRAWN / TRACED / CHECKED | | DMC 015 |




| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | C.M.I. | SCALE | PASSED | DATE |
| | SLAVE MUSIC KEYBOARD ASSEMBLEY | DRAWN / TRACED / CHECKED | | DRAWING NUMBER DMC005 |

MASTER MUSIC KEYBOARD COMPLETE

DRAWING REF.DMC004B

| REF.NO | PART NO | DESCRIPTION | REMARKS. |
|---|---|---|---|
| 01 | G0028 | COVER MUSIC WOOD BRIGE | |
| 02 | G0027 | PANEL MUSIC BASE BRIGE | |
| 03 | H0114 | SCREW 6GX1/2" PAN | |
| 04 | H0127 | SCREW 4BAX3/4" CHD | |
| 05 | H0008 | WASHER 4BA STAR | |

MASTER MUSIC KEYBOARD ASSEMBLY

DRAWING REF. DMC004.

| REF.NO | PART NO | DESCRIPTION | REMARKS. |
|---|---|---|---|
| 01 | G0027 | PANEL MUSIC K/BD BASE | |
| 02 | MC015 | KEYBOARD MECHAISM ASSY | |
| 03 | G0023 | CHEEK LH MASTER | |
| 04 | G5406 | BEZEL WHITE | |
| 05 | G5407 | LAMP | |
| 06 | G5404 | SWITCH #1 | |
| 07 | G5405 | SWITCH #2 | |
| 08 | G5146 | KNOB SLIDER POT | |
| 09 | G0105 | STRIP CLAMP MUSIC K/BD | |
| 10 | H0211 | NUT SWITCH | |
| 11 | G0024 | STRIP SLIDER POT | |
| 12 | G5161 | POT SLIDER | |
| 13 | G0025 | CHEEK RH MASTER | |
| 14 | G5165 | BEZEL DISPLAY RED | |
| 15 | MCMI12 | CARD MUSIC DISPLAY | |
| 16 | G5142 | SPACER 6BAX1/4" ROUND | |
| 17 | D6738 | CONNECTOR CANNON 7P | |
| 18 | D6710 | CONNECTOR CANNON 5S | |
| 19 | D6729 | CONNECTOR DMINI 25S | |
| 20 | D6727 | CONNECTOR DMINI 9S | |
| 21 | D6728 | CONNECTTOR DMINI 9P | |
| 22 | G5122 | CLIP CABLE | |
| 23 | D6731 | LUG DMINI | |
| 24 | MCMI10 | CARD C.M.I-10 | |
| 25 | G5219 | CONNECTOR UTH9356-6R | |
| 26 | MC070 | CABLE SLIDER POT ASSY | |
| 27 | MC063 | CABLE KEYBOARD ASSY | |
| 28 | MC071 | CABLE REAR PANEL | |
| 29 | G5107 | STANDOFF | |
| 30 | H0125 | SCREW 6GX1/4" CHD | |
| 31 | H0124 | SCREW 6BAX1/4" CHD | |
| 32 | H0117 | SCREW 6BAX1/4" CSK | |
| 33 | H0130 | SCREW 6BAX3/16" CSK | |
| 34 | H0012 | WASHER 6BA STAR | |
| 35 | H0201 | NUT 6BA HEX | |
| 36 | G5183 | FOOT RUBBER | |
| 37 | H0112 | SCREW 4BAX3/8" CHD | |
| 38 | H0008 | WASHER 4BA STAR | |

MUSIC KEYBOARD SUB-ASSEMBLY

DRAWING REF.DMC015

| REF.NO | PART NO | DESCRIPTION | REMARKS. |
|---|---|---|---|
| 01 | G5156 | KEYBOARD MUSIC 73 KEYS | |
| 02 | G5154 | BRACKET A/N/ K/BD MTG | |
| 03 | G5153 | BAR PLATED | |
| 04 | G5187 | RETAINER SPRING MUSIC K/BD | |
| 05 | G5158 | SPRING KEYBOARD MUSIC | |
| 06 | MCM11A | CARD K/BD MUSIC 24SW | |
| 07 | MCM11B | CARD K/BD MUSIC 25SW | |
| 08 | H0122 | SCREW 6BAX3/4" CHD | |
| 09 | H0012 | WASHER STAR 6BA | |
| 10 | H0201 | NUT 6BA HEX | |

SLAVE MUSIC KEYBOARD ASSEMBLY

DRAWING REF.DMC005

| REF.NO | PART NO | DESCRIPTION | REMARKS. |
|---|---|---|---|
| 01 | G0030 | COVER MUSIC SLAVE WOOD BEIGE | |
| 02 | G0029 | PANEL MUSIC SLAVE BASE BEIGE | |
| 03 | G5156 | KEYBOARD MUSIC 73 KEYS | |
| 04 | G0105 | STRIP CLAMP MUSIC K/BD. | |
| 05 | G0002 | CHEEK SLAVE LH B/K | |
| 06 | G0003 | CHEEK SLAVE RH B/K | |
| 07 | MC014 | SLAVE KEYBOARD INTERFACE CARD | |
| 08 | MC019 | CABLE MUSIC SLAVE K/BD INTERNAL | |
| 09 | G5183 | FOOT RUBBER | |
| 10 | G5122 | CLIP CABLE | |
| 11 | H0122 | SCREW 6BAX3/4" CHD | |
| 12 | H0117 | SCREW 6BAX1/4" CSK | |
| 13 | H0124 | SCREW 6BAX1/4" CHD | |
| 14 | H0112 | SCREW 4BAX3/8" CHD | |
| 15 | H0114 | SCREW SELF TAPPER NO6X1/2" SLOTTED PAN HEAD | |
| 16 | H0012 | WASHER 6BA STAR | |
| 17 | H0007 | WASHER 4BA FLAT | |

# S E R V I C E  M A N U A L

for

FAIRLIGHT

ALPHA/NUMERIC KEYBOARD #MC003

JUNE 1982.

REVISION 1

TABLE OF CONTENTS.

# 1.INTRODUCTION.

The FAIRLIGHT Intelligent Alpha-Numeric Keyboard has been designed to be used as the primary input console for the Fairlight range of microcomputers. It has 64 keys, which include all the usual 'typewriter'functions plus cursor control keys.

It is a completely self-contained unit using a microprocessor for maximum flexibility and adaptability for custom applications. By changing the 2708 EPROM in the keyboard, any special key function can be programmmed.

High-reliability Hall-Effect switches are used which means no contact wear. The keytops are of a 'double-shot'moulded type, giving permanent keytop legends which will not wear away.

Connection between the keyboard and the computer is made via a 7-core cable. This cable provides power to the keyboard plus the serial link between the two devices.

## 2.SPECIFICATIONS.

| | |
|---|---|
| Switch Module Type: | Hall-Effect(no contact wear) |
| Total ket travel: | 4.1mm |
| Key actuating force: | 71grams |
| Reliability: | 100,000,000 opertions/station |
| Keytop type: | Double-shot moulded |
| Data format: | RS-232C ASCII format |
| Baud rate: | 110 to 9600.Factory set to 9600 |
| Power requirements: | +16 to 18 volts at 500mA<br>-16 to 18 volts at 100mA |
| Connector type: | 9 pin 'D Mini' socket |
| Dimensions: | 415mm(W)x75mm(H)x170mm(D) |
| Weight: | 2.75kg |

# 3.FUNCTIONAL DESCRIPTION.

## 3.1 MPU,Decoding,RAM,Restart,Interupt clock and Option switches, (refer to drawing #IKB1-01).

### 3.1.1 Microprocessor Unit.

All keyboard functions are performed by the 6802 microprocessor unit (MPU) at location D2. This is activated by the 3.840MHz crystal which results in a MPU cycle time of 1.04 microseconds. At power-up the MPU is held reset by the 555 IC at location H2, to satisfy the 6802's reset requirements. After reset the MPU obtains its restart vector from ROM 2 at location C1 and starts program execution.

The 6802 MPU contains 128 bytes of internal RAM. This is permanently enabled by tying the Ram Enable signal(pin 36) high. This is the only RAM in the keyboard.

### 3.1.2 Address Decoding.

Selection of both ROMs, the Option switch and the PIA is performed by the LS139 1-of-4 decoders at location B1. The devices are selected when the devices' address(s) is on the address bus and both VMA and E are active (high). Not all address lines are used in the decoding so the devices appear in several places in the 6802's address space. See the following address map.

The address map of the keyboard is as follows:

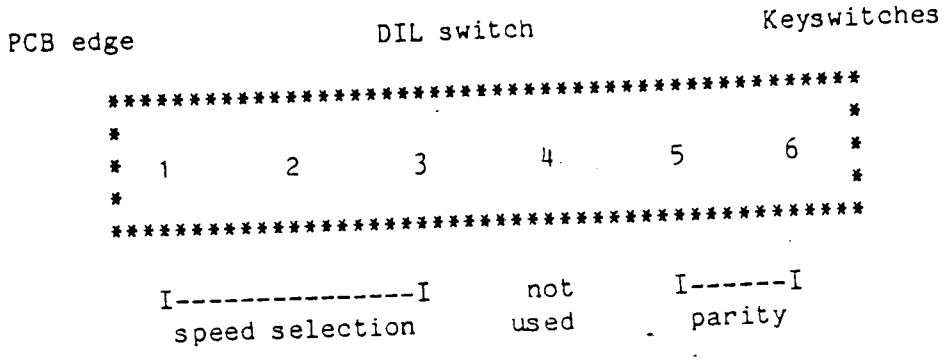
| Address ( Hex ) | Function |
|---|---|
| 4000-7FFF | Option switch |
| 8000-BFFF | PIA |
| C800-CBFF | ROM 1 (optional) |
| CC00-FFFF | ROM 2 |

Restart and other vectors must be stored in the last locations of ROM 2.

### 3.1.3 Software Readable Switch

The six-pole dual-in-line (DIL) switch provides for the selection of baud rate and parity, as follows :-

0 refers to switch on (closed).
1 refers to switch off (open).




3.1.4 DIL Switch selection

Speed selection (baud)

| 1 | 2 | 3 | |
|---|---|---|---|
| 0 | 0 | 0 | 9600 |
| 0 | 0 | 1 | ~~4800~~ 600 |
| 0 | 1 | 0 | 2400 2400 |
| 0 | 1 | 1 | ~~1200~~ 150 |
| 1 | 0 | 0 | ~~300~~ 4300 |
| 1 | 0 | 1 | ~~110~~ 300 |
| 1 | 1 | 0 | ~~110~~ 200 |
| 1 | 1 | 1 | 110 |

Parity selection

| 5 | 6 | |
|---|---|---|
| 0 | 0 | even parity |
| 0 | 1 | odd parity |
| 1 | 0 | no parity bit 7 set to 0 |
| 1 | 1 | no parity bit 7 set to 1 |

The standard switch setting is:

| 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|
| on | on | on | on | on | off |

3.1.5 Interrupt Clock

The 6802's E output is divided by 100 by the dual CMOS counter 4518 at location A2 to provide a 9.6kHz interrupt source. This clock is connected to the PIA's CA1 pin which in turn is programmed to generate an interupt to the MPU. This is used by the software in determining the serial output baud rate.

3.2 PIA, Voltage Regulation, Clicker and RS-232 signal generation. ( refer to drawing #IKB1-02).

3.2.1 Parallel Interface Adapator (PIA).

The two 8 bit ports in the PIA at location D1 are used to scan the keyswitch matrix. The remaining lines are used to generate RS-232 controls and the data line. The ports and control line functions are as follows:-

| | |
|---|---|
| Port A | input, from keyswitch columns |
| Port B | output,to keyswitch rows |
| CA1 | input,recieves 9.6kHz clock |
| CA2 | output,CTS flag |
| CB1 | input,RTS flag |
| CB2 | output,keyboard data |

3.2.2 Voltage Regulation.

The keyboard recieves +/- 20 volts from the main computer's power supply along the same cable as the keyboard's data signals. These voltages are regulated to -12,-5,+12 and +5 by the three terminal regulators in locations VR1,VR2,VR3 and VR4 on the heat sink along the edge of the PCB respectively. A 10 ohm 5 watt resistor is in series with the +20 volts and the 7812 +12 volt regulator to reduce the power dissipation in the regulator.

3.2.3 Clicker.

The audible feed back in the keyboard is provided by a relay driven by a discret monostable. The monostable is triggered by any serial output data. This monostable is configered around the CMOS 4001 at location G2 and capacitors C15,16 and resistors R6,7 . A LED is conected across the relay and flashes when the relay is activated.

3.2.4 RS-232 Levels.

The TTL signal outputs are converted to RS-232 levels by the driver in location H1 and inputs are converted to TTL by attenuators feeding LS14 inverters in location F1.

3.3 Keyboard operation.

The keyboard is scanned by the MPU by setting successive rows to "1" using the PIA, and seeing if any columns go to "0". Each key has a unique row and column number thus allowing the MPU to access each of the 64 keys individualy.

The HALL EFFECT keyswitches do not "bounce", so repetitive reads of a depressed key do not have to be made to distinguish if a key is pressed or released. The keyboard scanning is the main program loop. When keys are found depressed and later released, their state is noted in a 64 bit 'key state' table and the appropriate ASCII code is looked up, taking into account any other simultaneous depression of keys (such as shift or control). The character to be sent is put in a queue. One key can be handled each scan.

The characters in this queue are then outputted, one bit at a time in the interrupt routine. The transmission rate is determined by the setting of the option switch and the 9.6kHz interrupt clock. This results in N key roll-over.

4.1.Bottom Cover Removal.

1. Disconnect the Power/Signal cable from the computer before proceding.

2. Place keyboard face down on smooth surface.

3. Using 'locking type' bladed screwdriver,remove the 4 screws from the base cover. Access is gained through the 4 clearance holes in the bottom cover.

4. Lift off the cover and slide the cord grip out from the bottom cover cut-out.

4.2.Cable Removal.

1.Remove bottom cover as in 4.1.

2.Spread cord grip open to release cable.

3.Remove the cable from the Printed Circuit Card by spreading the connector locking lugs apart.

4.3.Printed Circuit Card Removal.

1.Remove bottom cover as in 4.1.

2.Leave keyboard laying face down, remove the 2 hexagon nuts and locking washers both both ends of the card.

3.Lift out the card from the top cover.

4.4.EPROM upgrade.

1.Remove the Printed Circuit Card as in 4.3.

2.Place the card down on a flat surface with the keytops facing upwards.

3.Locate the EPROM near the heatsink bracket, refer to exploded view drawing #DMKB2.

4.NOTE THE POSITION OF PIN 1 ON THE EPROM WITH RESPECT TO ITS SOCKET BEFORE REMOVING THE EPROM. Carefully lift out the EPROM from its socket.

5.To replace the EPROM, position its pins over its socket *NOTE POSITION OF PIN 1 BEFORE INSERTING* and push-down on the EPROM until its bottom is sitting flat on its socket.

4.5. Keyswitch Module Removal.

1.Remove the bottom cover as in 4.1.

2.Remove the keytop from the module being replaced and as many adjacent buttons as required to allow adequate workingspace. The keytop can be removed by pulling or prying upward with a padded tool from their under side. FAIRLIGHT INSTRUMENT recommends to use the 'Keytop Puller'tool,(Part #SW-10485). Refer to figure 1.

3.Unsolder the 4 terminals of the lead frame package from the PCB using a temperature contorlled soldering iron set to 750F degrees.Use a solder removal tool to remvove all the solder from the pin hole in the PCB. Refer to figure 2.

4.Insert the 'Module Removal 'tool,(Part #SD-10101)at each end of the module.With the Module Removal tools in position, grip the switch module with a pair of pliers and pull straight out.Refer to figure 4.

5.Replace the module with same part number type as the one being replaced.

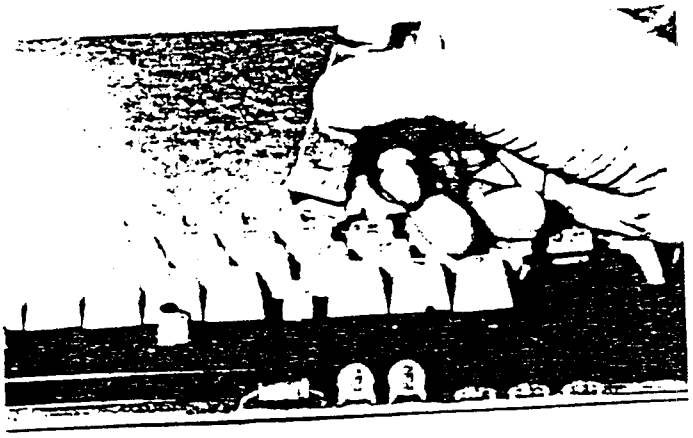


Figure 1. Button Removal

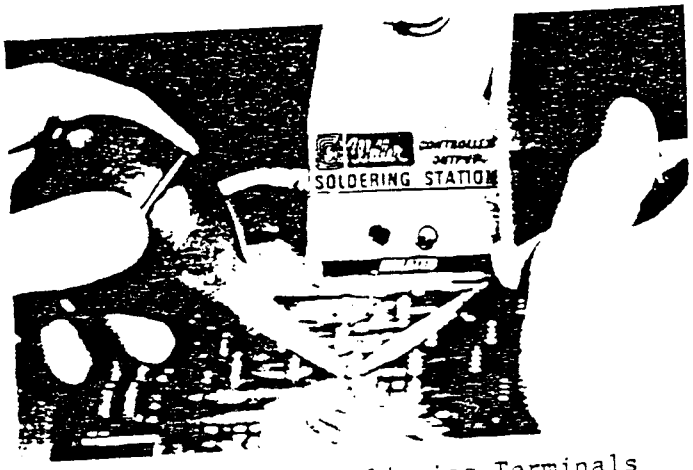



Figure 2. Unsoldering Terminals

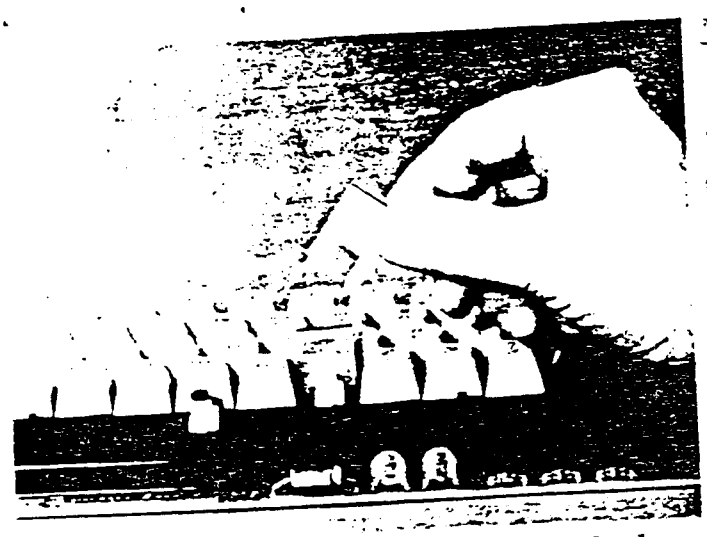


Figure 3. Inserting Removal Tools

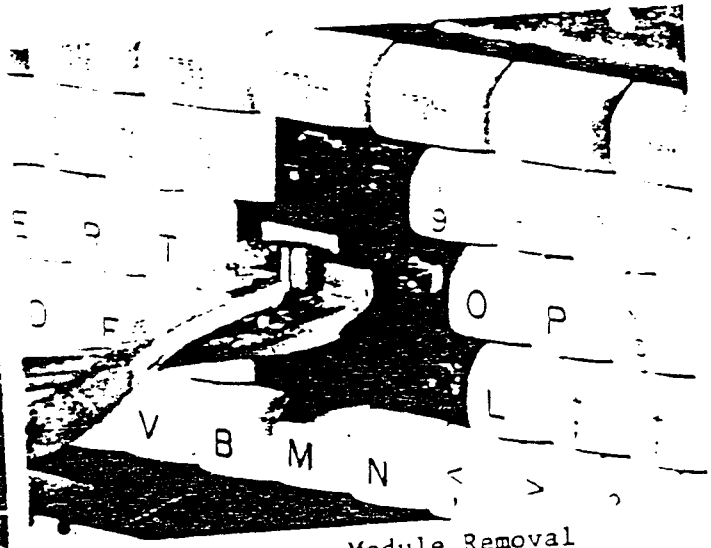
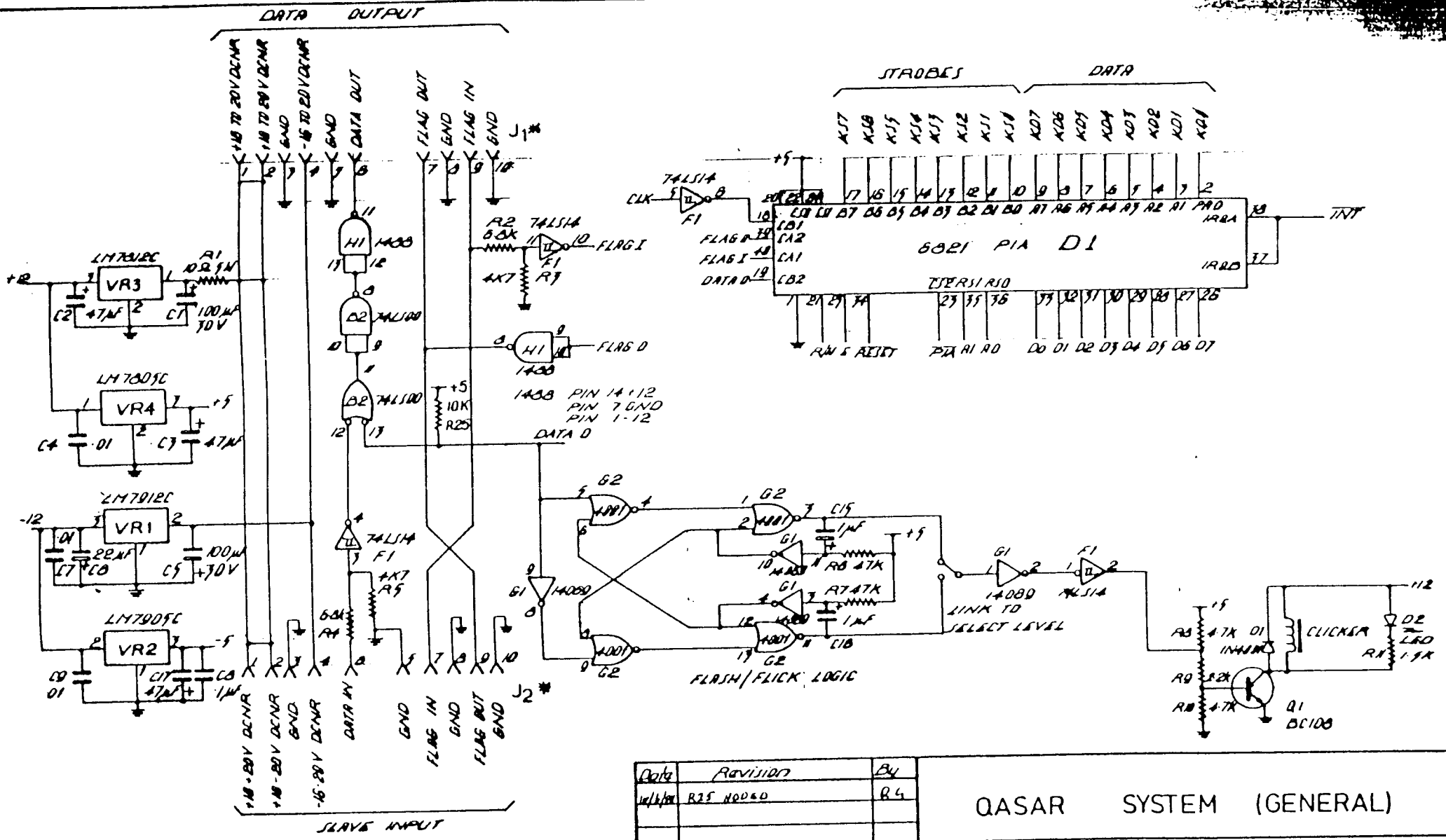



Figure 4. Module Removal




* CONNECTOR PINS ON $J_1$ + $J_2$ ARE NUMBERED ACCORDING TO POSITION IN 10 WAY STRIP CABLE. PIN 1 ON ARROW END OF CONNECTOR

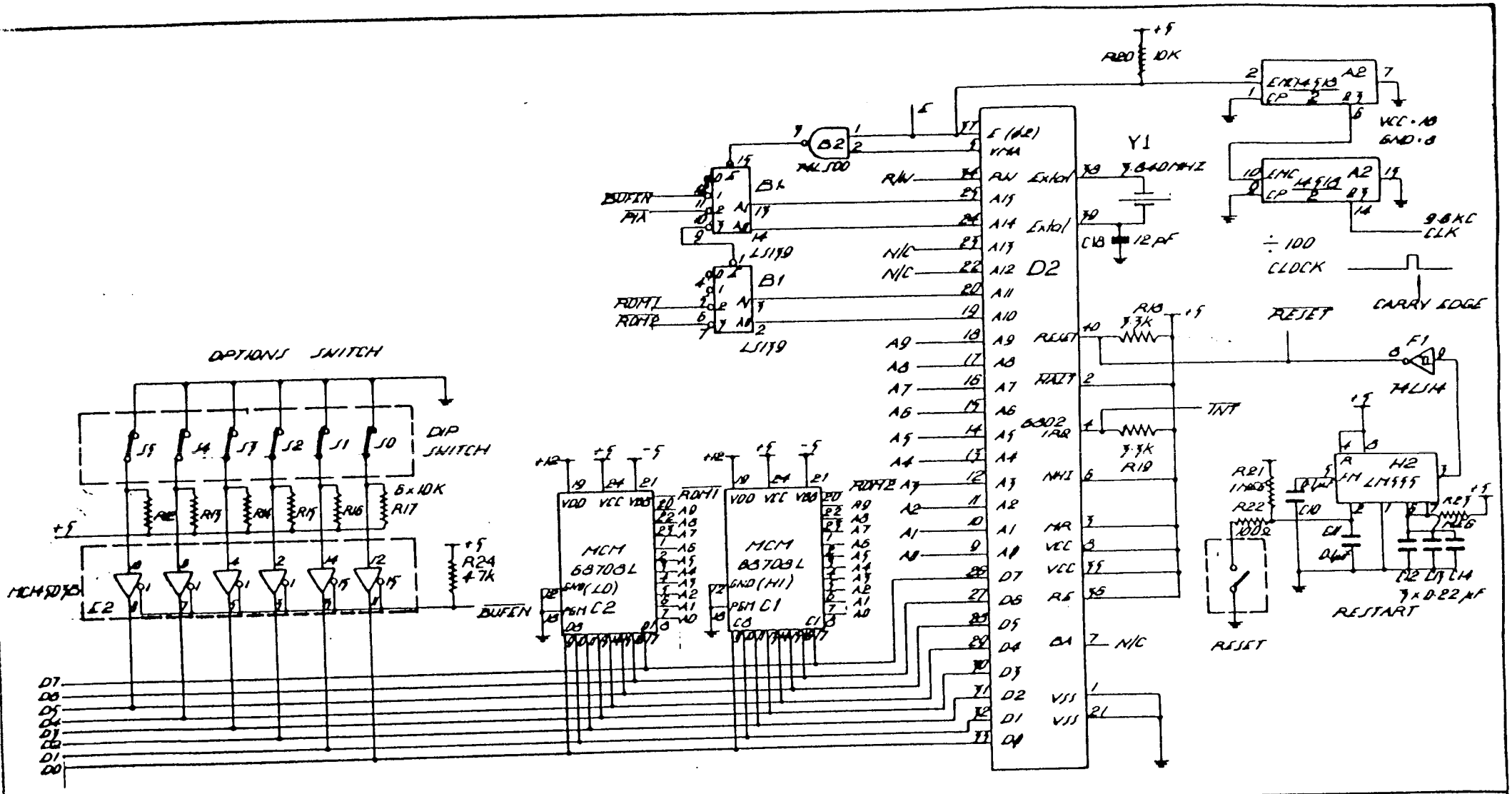
| Date | Revision | By |
|---|---|---|
| 10/11/81 | R25 MODED | RG |

# QASAR SYSTEM (GENERAL)

## INTELLIGENT KEYBOARD UNIT
## DATA PORTS & MISCELLANEOUS LOGIC

Sheet 2 of

| Drawn | Checked | Scale | Drawing N° |
|---|---|---|---|
| BINOPI Pty | P.V. | NIL | IkB1 – 02 |
| NOV 1981 | | | |




NOTES: 1. SWITCHES MUST BE TTL COMPATABLE TYPES.
2. IN SINGLE ROM SYSTEMS SHUT "40" ROM

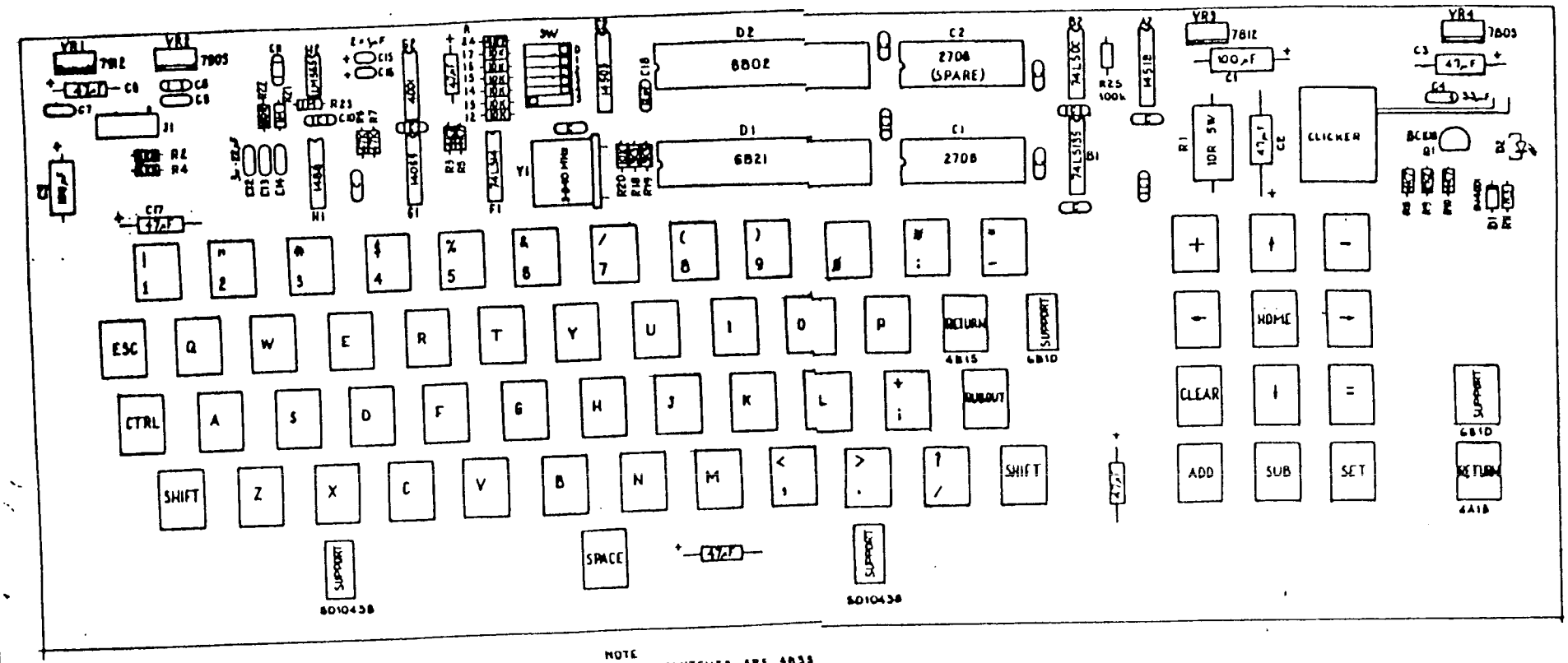
| Issue | Revision | By |
|---|---|---|
| 10/4/81 | S26, C18 ADDED | GG |

# QASAR SYSTEM (GENERAL)

## INTELLIGENT KEYBOARD UNIT PROCESSOR (ROM) OPTIONS

Sheet 1 of 3

| Drawn | Checked | Scale | Drawing No. |
|---|---|---|---|
| RINOPL Pty | P.V. | | KB1 01 |




NOTE
ALL SWITCHES ARE 4B33
UNLESS SPECIFIED OTHERWISE

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REM. |
|---|---|---|---|---|
| FAIRLIGHT INSTRUMENTS P/L<br>15 BOUNDARY ST RUSHCUTTERS BAY 2011 | | SCALE | | PAGE 80 |
| ALPHA [illegible] KEYS<br>INTELLIGENT [illegible] | | DRAWN | B.G. | IKE |
| | | TRACED | B.R.L. | |
| | | CHECKED | R.V. | |

# 7.ELECTRICAL PARTS LIST.

## 7.1 IKB1. Alpha/Numeric Intelligent Keyboard Card.

### IC'S

| Circuit Ref. | Type | Description | Circuit Ref. | Type | Description |
|---|---|---|---|---|---|
| A2 | 4518 | DUAL COUNT. | E2 | 4503 | HEX TRI.BUFFER |
| B1 | LS139 | DUAL DECODER | F1 | LS14 | HEX SCH.INVERT |
| B2 | LS00 | QUAD NAND | | | |
| | | | G1 | 4069 | HEX INVERT. |
| C1 | 2708 | 1K EPROM | G2 | 4001 | QUAD NOR |
| D1 | 6821 | PIA | H1 | 1488 | QUAD DRIVER |
| D2 | 6802 | PROCESSOR | H2 | 555 | TIMER |
| VR1 | 7912 | -12V REG. | | | |
| VR2 | 7905 | -5V REG. | | | |
| VR3 | 7812 | 12V REG. | | | |
| VR4 | 7805 | 5V REG. | | | |

### TRANSISTORS

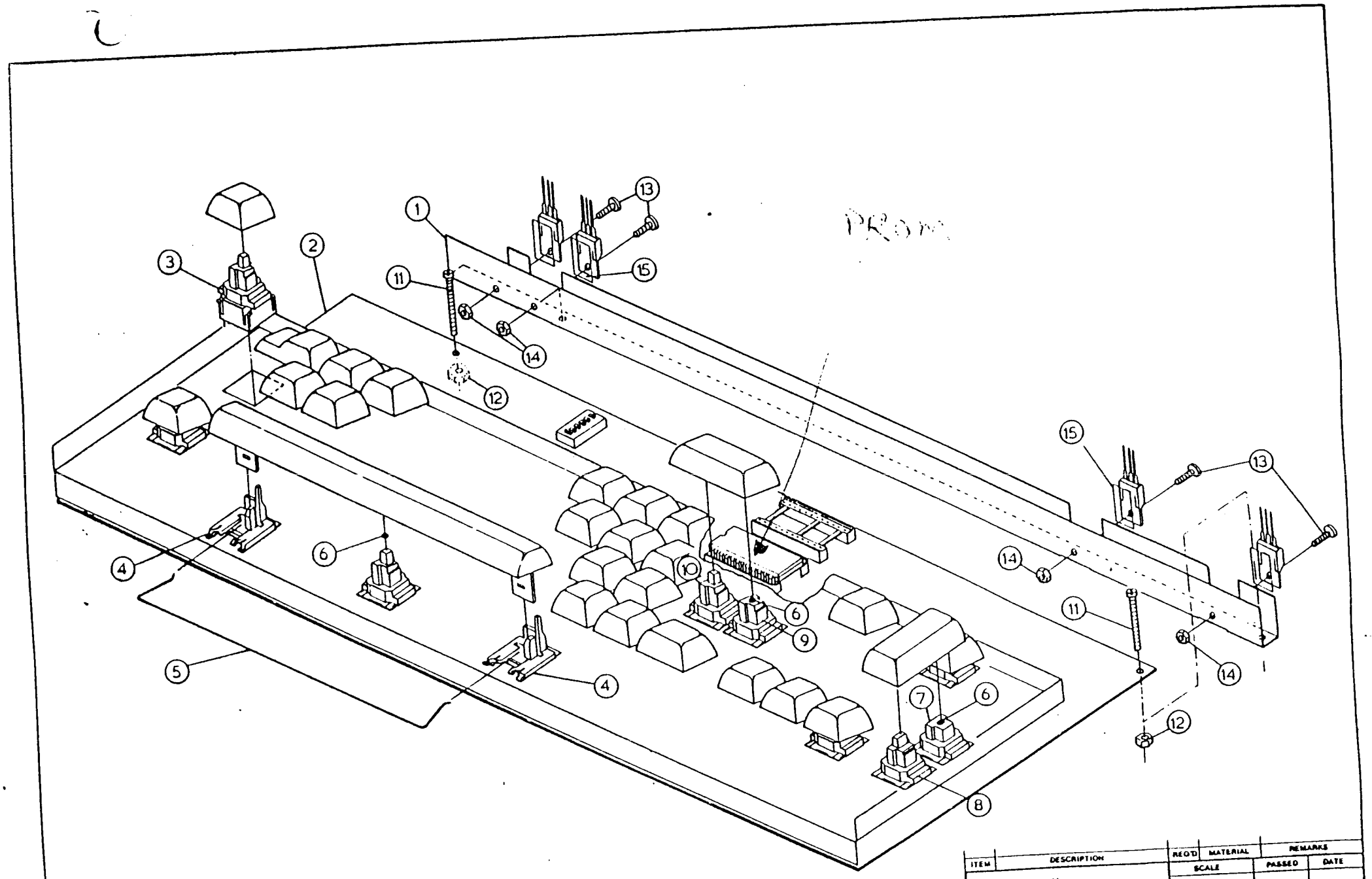
| | | |
|---|---|---|
| Q1 | BC108 | TRANSISTOR |

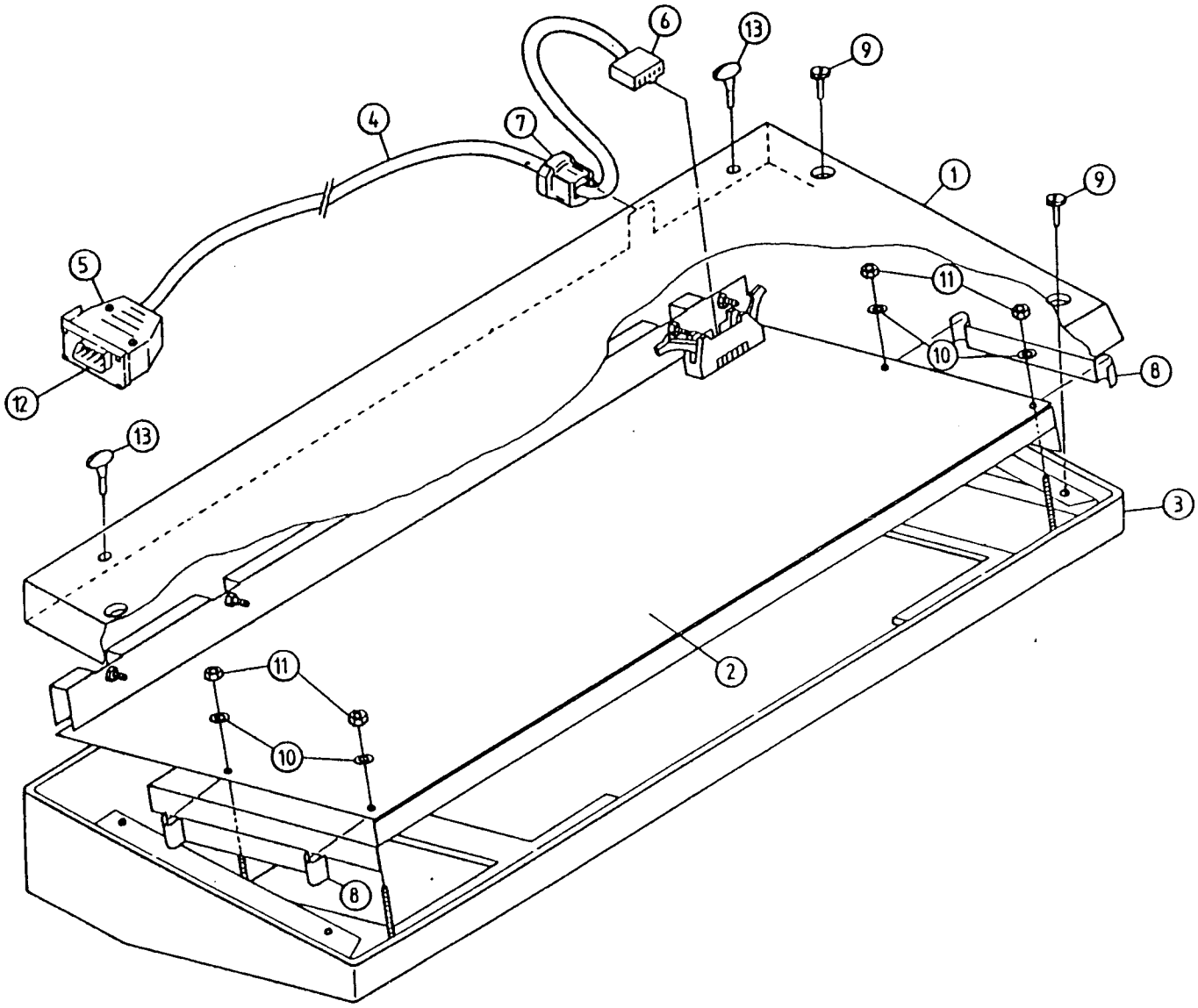
### DIODES

| | | |
|---|---|---|
| D1 | 1N4401 | DIODE |
| D2 | LED | RED 3mm |

### RESISTORS

| | | | | |
|---|---|---|---|---|
| R1 | 10R | 5 WATT | R11 | 1K5 |
| R2 | 6K8 | | R12-17 | 10K |
| R3 | 4K7 | | R18,19 | 3K3 |
| R4 | 6K8 | | R20 | 10K |
| R5 | 4K7 | | R21 | 1M |
| R6,7 | 47K | | R22 | 100R |
| R8 | 4K7 | | R23 | 1M |
| R9 | 2K2 | | R24 | 4K7 |
| R10 | 4K7 | | R25 | 10K |






| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS | |
|---|---|---|---|---|---|
| | | SCALE | | PASSED | DATE |
| | CM1 | | | | |
| | ALPHA/NUMERIC KEYBOARD ASSEMBLY | DRAWN | | | DRAWING NUMBER DMC 003 |
| | | TRACED | | | |
| | | CHECKED | | | |

# 9.MECHANICAL PARTS LIST.

## 9.1 DMKB2 Alpha/Numeric Keyboard Module.

| Drawing ref. | Part #. | Description. |
|---|---|---|
| 1 | G1046 | Heatsink |
| 2 | EQKB1 | PCB |
| 3 | G0042 | Switch Module 4B3S |
| 4 | G4008 | Support Module SD10438 |
| 5 | G4009 | Tension bar |
| 6 | G0061 | Felt pad |
| 7 | G4006 | Switch Module 6A1D |
| 8 | G4005 | Switch Module 4A1S |
| 9 | G4004 | Switch Module 6B1D |
| 10 | G4003 | Switch Module 4B1S |
| 11 | H0123 | Screw 6BAx1" CHD |
| 12 | H0201 | Nut 6BA Hex. |
| 13 | H0110 | Screw 4BAx1/4" nylon |
| 14 | H0202 | Nut 4BA Hex. |
| 15 | H0002 | Washer Mica TO220 |

## 9.2 DMC003 Alpha-Numeric Keyboard Assembly.

| | | |
|---|---|---|
| 1 | G1049 | Bottom cover |
| 2 | MQKB1 | Card assembly |
| 3 | G1017 | Top cover |
| 4 | MC013 | Cable assembly |
| 5 . | D6753 | Cover assembly D-Mini |
| 6 | D6021 | Connector shell 10Way |
| 7 | G5215 | Cord grip |
| 8 | G1048 | Spacer |
| 9 | H0112 | Screw 4BAx3/8" CHD. |
| 10 | H0008 | Washer 4BA Star |
| 11 | H0202 | Nut 4BA Hex. |
| 12 | D6753 | Connector 9 pin D-Mini |
| 13 | G5180 | Rubber foot |

TABLE OF CONTENTS

## 1.SAFETY WARNING

CAUTION: Unqualified persons should not attempt repair or adjustment to this equipment. High voltages present inside the unit.

### 1.1 Picture tube Handling

A large amount of mechanical potential energy is stored in the picture tube by virtue of its vacuum.

The strength of the glass envelope will be impaired by surface damage, such as scratches or bruises (localised surface cracks caused by impact). When a tube is not in its equipment or original packing, it should be placed faceplate downwards on a pad of suitable ribbed material which is kept free from abrasive substances. Stress on the neck of the tube must be avoided. Handle by the following methods:-

A)Tube on one edge

To lift a tube from the edge down position, one hand should beplaced around the parabola section of the cone and the other hand should be placed near (slightly below) the centre of the faceplate as shown in Figure 1.
UNDER NO CIRCUMSTANCES SHOULD ANY FORCE BE APPLIED TO THE NECK

B)Tube face-down

To lift a tube from the face-down position, the hands should be placed under the areas of faceplate close to the fixing lugs at diagonally opposite corners of the faceplate as shown in Figure 2. The tube must not be lifted from this position by the lugs themselves.
UNDER NO CIRCUMSTANCES SHOULD ANY FORCE BE APPLIED TO THE NECK OF THE TUBE.

C)Tube face-up

To lift a tube from the face-up position, the hands should be placed under the areas of cone close to the fixing lugs at diagonally opposite corners of the cone as shown in Figure 3. The tube must not be lifted from this position by the lugs themselves.UNDER NO CIRCUMSTANCES SHOULD ANY FORCE BE APPLIED TO THE NECK OF THE TUBE.

If the handling procedures for the tube prior to insertion in the chassis is such that there is a risk of personal injury as a consequence of accidental damage to the tube, then it is recommended that protective clothing should be worn particularly eye shielding.

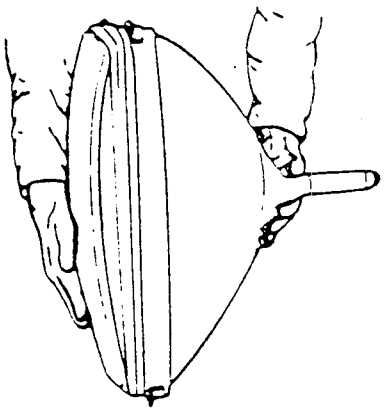


Fig.1 – Lifting picture tube from edge-down position

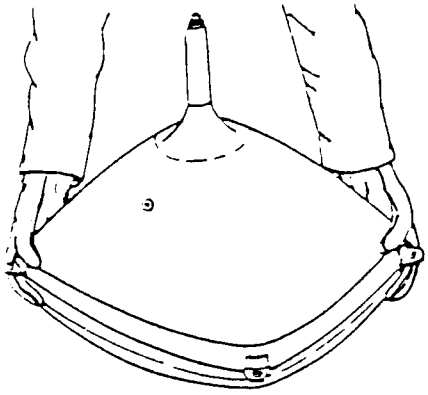


Fig.2 – Lifting picture tube from face-down position

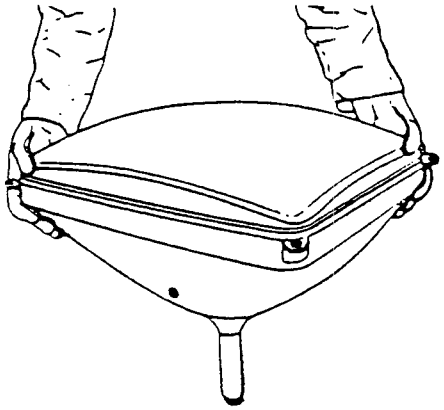


Fig.3 – Lifting picture tube from face-up position

Attention is called to the fact that high voltage may be carried by the internal conductive coating which is connected to the final anode connector and also by the external coating if not earthed, even after the tube has been removed from the unit. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts).

## 2.SPECIFICATIONS

| | |
|---|---|
| Picture tube type: | 15inch P31 green phospher with anti-reflective bonded face-plate. 110 degree deflection angle. |
| Video Response(Typical): | 5Hz to 20MHz(-3db) |
| Video output risetime(Typical): | 30V in 18nS |
| Horizontal Linearity: | better than 3% |
| Field Linearity: | better than 1.5% |
| Geometric rasterdistortion: | with 1% |
| Scanning frequency: | Horizontal:15,625Hz<br>Vertical:50Hz |
| Horizontal Flyback time: | 10.5uS |
| Horizontal blanking time: | 10.5uS |
| Field blanking time: | 800uS |
| Anode voltage (eht): | 17KV at zero beam current |
| Input Signal: | 1V pk-pk composite video (negative sync) 75ohms |
| Controls:- | |
| External: | a)Contrast, Brightness |
| Internal: | a)H.frequency, H.phase Dynamic focus, width & H. linearity.<br>b)V.frequency,height & V. linearity.<br>c)Video black level.<br>d)24V supply adjust. |
| Power Requiements: | 100V,120V,220V,240V -5% +10% 50Hz - 60Hz |
| Power Consumptions: | 35W (nominal) |
| Dimensions: | 490mm(W) x 345mm(H) x 380mm(D) |
| Weight: | 30kg |

## 3. INTRODUCTION.

The FAIRLIGHT Graphics Monitor is a high resolution CRT monitor for use with the Fairlight range of microcomputers. It is designed to accept composite video from the Graphics card located in the microcomputer.

The display tube is a high-resolution 15" diagonal P31 type which gives a crisp, green image. The large format results in a highly readable display, which means low operator fatigue.

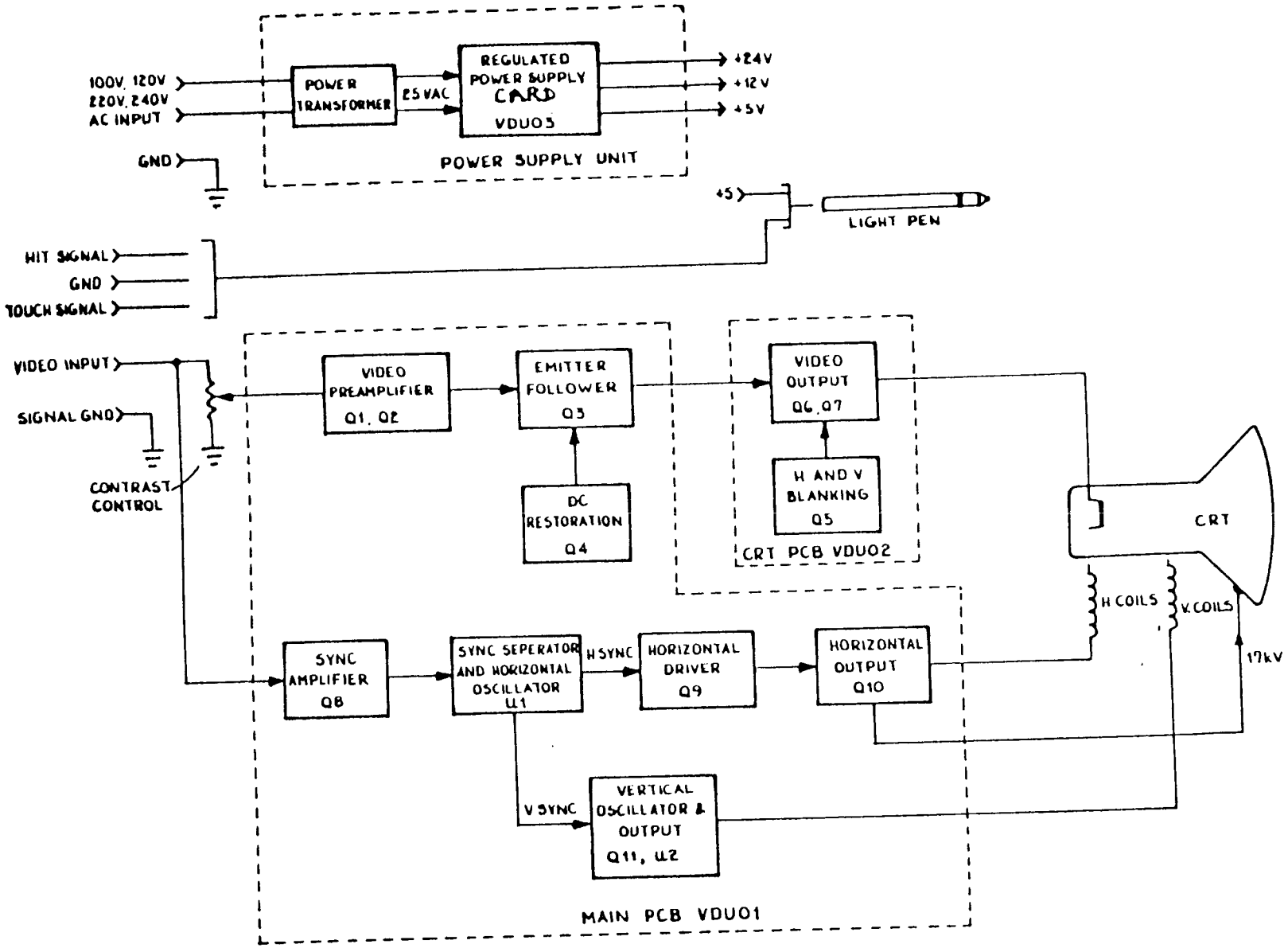
An optional high-performance Light Pen is used with the monitor. The lightpen is used for inputting graphical data, selecting options from a menu or cursor positioning in word-processing.

The lightpen is of high quality metal construction for a pleasant "feel". Connection to the monitor is by means of a flexible spiral retractable cord and miniature connector.

When the pen is pointed at the screen, a bright cursor is displayed to show the exact point it is 'seeing'. The pen is activated by touching the end with a finger, at which time a T.T.L. 'Touch' signal is sent to the computer.

A single cable, containing 3 co-ax cabl, makes the signal connection between the monitor and computer.It carries the video information from the computer plus the Light Pen HIT and TOUCH signals back to the computer.Mains power for the monitor is supplied via the computer, to allow the mains keyswitch to turn both Monitor and computer On and Off together.

A block diagram of the Graphics Monitor is shown on Page 5.




BLOCK DIAGRAM OF GRAPHICS TERMINAL MQ215L

## 5. CIRCUIT ADJUSTMENT.

### 5.1. Preliminary set-up.

1. Check that mains selector on rear of Graphics Monitor is selected to suit local mains voltage.
2. Apply 1V pk-pk composite video signal.
3. Connect mains supply.
4. Adjust contrast and brightness controls for optimum picture.

### 5.2 Power Supply Card(VDU03)

#### 5.2.1 24V adjust.

1.Connect a voltmeter to pins 3 and 1 on connector P9 on the power supply card VDU03.
2.Check output is +24V DC.
3.Adjust using RV1, if necessary.

### 5.3 Main Card (VDU01)

#### 5.3.1 Horizontal Frequency.

1.Short point 'fo' (refer to circuit diagram) to ground.
2.Adjust H. freq control VR3 for near stable picture.
3.Remove shorting strap from 'fo'.

#### 5.3.2 H. Phase.

1.Increase brightness control until picture background can be seen.
2.Adjust H. Phase control VR4 to centre picture horizontally within background raster.

#### 5.3.3 Width.

1.Adjust Width Coil L4 to obtain approx. 15mm gap between raster and edge of screen at the vertical centres.

#### 5.3.4 H. Linearity.

1.Adjust H. Lin coil L2 to obtain optimum horizontal linearity at the start and end of the horizontal scan.
2.Readjust Width Coil L1 if necessary.

#### 5.3.5 Vertical Frequency.

1.Turn V. Frequency control VR5 until picture starts rolling down the screen and the blanking bar is seen.
2.Slowly turn VR5 back so that bar rolls up and locks in.
3.Turn VR5 a few more degrees to ensure stable locking.

5.3.6 Vertical Height & Linearity.

1.Increase picture brightness until background raster can be seen.

2.Turn V. Height control VR7 until there is approximately 15mm gap between raster and edge of the screen at the horizontal centres.

3.Adjust V. Lin control VR6 for optimum vertical linearity at the top and bottom portions of the picture.

4.Repeat step 2. if necessary.

5.3.7 Focus Adjustment.

1.Adjust contrast and brightness controls for optimum picture.

2.Adjust Focus control VR9 for optimum picture focus.

5.4 CRT Card VDU02.

5.4.1 Black Level

1.Turn contrast control to maximum.

2.Check video level at pin 5 of P4 is approx. 4.5V pk-pk composite video.

3.Monitor collector of Video output transistor Q6 with oscilloscope.

4.Set black level of video to +60V using black level controlVR2.

# 6. DISASSEMBLY.

6.1 Top Cover Removal (Refer to Exploded View #MQ215L/02)

1.Remove the 4 counter-sunk screws marked 6 from both sides of cover.

2.Remove the 3 dome headed screws marked 7 from the rear panel.

3.Lift off top cover.

6.2 Picture tube Replacement. (refer to Exploded View #MQ215L/01)

Caution: Refer to SAFETY WARNING Section 1 before proceeding.

1.Remove light pen as in 7.4.1.

2.Remove top cover as in 6.1.

3.Remove 10way cable from the VDU03 P.C.B.

4.Disconnect the red high voltage cable from the picture tube and discharge tube.

5.Remove the CRT P.C.B. VDU03 and defletion yoke from the neck of the picture tube.

6.Remove the six cheese-head screws holding the front panel/CRT brackets, marked 16 on drawing.

7.Tilt Front panel forward and down until face of the picture tube is laying face down in front of Graphics monitor

8.Remove 4 outer hexagon nuts and washers from front panel studs, and slowly withdraw picture tube from front panel.

# 7.LIGHT PEN.

## 7.1 General description.

The light pen is completely self-contained and requires only a 5V supply. The pen is activated by touching the end with a finger, at which time a T.T.L. touch signal is sent to the computer. The 'touch' signal only with the 'hit' signal is connected to the computer via the 5 pin Cannon connector located on the rear of the V.D.U. 5V for the light pen is obtained from the P.S.U. card located on the Power Supply Unit (refer to Section 8).

## 7.2 Light Pen Adjustments.

### 7.2.1 Sensitivity.

The pen sensitivity is factory set, to provide good performance in most applications. If necessary, the sensitivity may be adjusted by inserting a screwdriver through the small hole in the body. CLOCKWISE rotation DECREASES the sensitivity. The pen may be set for maximum sensitivity (without a light source) by increasing the sensitivity until the pen free-runs and then backing off until the outputs disappear.

### 7.3.1 Operation check.

Operation of the pen may be checked by using a laboratory oscilloscope both as signal source and display. Set the scope for a line triggered sweep at a speed of one centimeter per uSec. Connect the vertical input to the pen light pulse output. When the tip of the pen is positioned over the trace a 1uSec pulse should appear about 300nSec to the right of the pen. Increasing the sensitivity should reduce the delay.

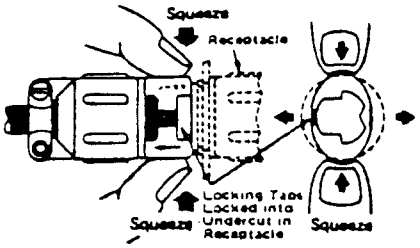
## 7.4 Light Pen Removal and Replacement.

The light pen connector is mated to the connector on the V.D.U. front panel via a locking type connector.

### 7.4.1 Removal.

The connector cannot be unmated until the sides of the plug are squeezed (Figure 1).

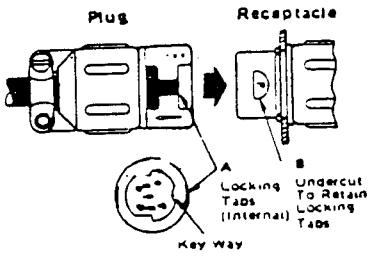
Light Pen Removal/Replacement.




**Don't Turn or Twist.**
**Don't use Hand Tools.**

1. Squeeze finger grips to flex plastic coupling area. The locking tabs will deflect outward and unlock.
2. Pull plug from receptacle.

Figure 1 - Removal.




1. Turn plug so "keyed" insulator faces align.
2. Push plug onto receptacle until locking tabs (A) snap into undercuts (B).

Figure 2 - Replacement.

7.4.2 Replacement.

Connection is made by pushing the plug on the light pen cardonto the connector on the VDU front panel until the locking tabs snap into the locked positon (Figure 2).

2 NOIR

3 VERT

CENTRE ROUGE

6 BLANC

# 8. POWER SUPPLY UNIT.

## 8.1 General Description.

< The power supply unit is located behind the front panel Light Pen cut-out. The unit consists of the power transformer, voltage selector switches and the regulated DC power supply card VDU03. The unit provides 24V and 12V for the Main Card VDU01 and 5V for the Light Pen.

A multi-tapped primary power transformer is used. It has low magnetic leakage to prevent picture tube interference. The secondary output is connected via 3 pin connector to the Power Supply Card.

## 8.2 Power Supply Card VDU03.

### 8.2.1 Circuit Description.

The bridge rectifier DB1 and the filter capacitors C1 and C2 provide the DC supply for the IC regulators U1 and U2. U1 is the adjustable regulator used for the 24V DC. Its output is factory adjusted to 24V using VR1 and should only need readjusting should U1 or its associated components be replaced.

DB1 also supplies DC to the 12V regulator U2. To reduce the power dissipation in the 12V regulator two 5.6V zener diodes are used in series. The 24V and 12V are connected to the VDU01 card via the 3 pin connector.

U2 also supplies 12V to the 5V regulator U3. U3 is used for the light pen supply and is connected via the 10 way connector where connections for the Light Pen's 'Hit' and 'Touch' signals are also made.

# 9. MAIN CIRCUIT BOARD VDU01.

## 9.1 General Description.

The main printed circuit card VDU01 is mounted vertically on the opposits side of the power supply unit. It generates all the picture tube supplies, provides the driving circuitry for the deflection coils and processes the video signal. Connections to the picture tube are made via the circuit board VDU02 which is mounted on its neck. This card has the video output amplifier, printed circuit board spark gaps and decoupling for the picture tube DC suplies.

## 9.2 Circuit description.

### 9.2.1 VIDEO PREAMPLIFIER

The video preamplifier (Q1,Q2) is designed to accept a 1 volt pk-pk video signal (negative sync) at 75 ohms. The 500 ohm contrast control is provided at the input and is padded with R1 to provide the proper cable termination.

### 9.2.2 D.C. RESTORATION

After the preamplifier, D1 and Q4 are used to provide the DC restoration at the base of Q3. DC restoration occurs during horizontal flyback. This is achieved by connecting the base of Q4, through R15 and D5, to the horizontal output transistor Q10.

The signal is now passed to the emitter follower Q3 where it is coupled to the video output stage (located on the VDU-02 P.C.B.) via a 5 way notched ribbon cable.

### 9.2.3 BLANKING

Q5 is the retrace blanking transistor. It is driven by the horizontal pulses derived from the line output transistor Q10. These positive pulses, along with the positive vertical blanking pulses from pin 4 of the vertical timebase IC (U2) are fed to the base of Q5 which turn it on, thus cutting off Q6 during vertical and horizontal retrace.

### 9.2.4 SYNC SEPERATOR AND HORIZONTAL TIMEBASE

The same video that is fed to the contrast control is fed to the sync amplifier Q8. After amplification the composite sync is connected to U1 via R29. This IC performs the functions of sync seperator, line oscillator and coincidence detector. The sync is fed to pin 9 via a waveform conditioning network. The

horizontal frequency is set by C17 and is adjustable by VR3.

Information for the coincidence detector is obtained from the horizontal output transistor Q10 via the H phase control VR4 and fed to pin 6. Adjustment of the mark-space ratio is effected by the voltage applied to pin 4. The horizontal driving pulses are obtained from pin 3 and are routed to the base of the driver transistor Q9. Vertical sync output is on pin 8, which via R57 is connected to the vertical IC U2.

9.2.5 HORIZONTAL DRIVER

Driver transformer Tx2 energised by Q9 generates the drive of required form and magnitude for the horizontal output transistor Q10. A non simultaneous mode is employed so that the driver transistor is conducting when the horizontal output transistor is cut-off. A 1.8 ohm series resistor R44 defines the forward base current of Q10, and a 68 ohm resistor R45 in parallel with the base-emitter junction prevents ringing voltages from turning the device on during flyback.

The network R41 and C26 across the primary of the driver transformer provides the required tuning and waveshaping. Decoupling for the whole driver stage is effected by R43, C52 and C53. R43 has a current limiting function in the event horizontal pulses are lost.

9.2.6 HORIZONTAL OUTPUT STAGE

The horizontal output stage basically consists of the horizontal output transistor Q10, deflection coil (connected between linearity coil L2 and the dynamic focus transformer Tx3) and the horizontal output transformer Tx1.

The horizontal timebase employs the series efficiency diode circuit (boost circuit) technique. A feature of this circuit is that the voltage developed across the boost capacitor C33 is added to the 24V DC supply and in this way about 63V is made available for direct drive of the line deflection coils. D8 is the series efficiency diode. The deflection coils are connected to the whole of the primary winding of the horizontal output transformer and in parallel with Q10, minimising the possibility of ringing during scan. The linearity correction and S correction is carried out by having the linearity coil L2 and capacitors C30 and C29 in series with the horizontal deflection coils. The width coil L1 provides adjustment of the scan amplitude of about ± 3%. Tx3 is the dynamic focus transformer.

9.2.7 PICTURE TUBE SUPPLIES

All the high voltage supplies for the picture tube are derived from the horizontal output transformer. The e.h.t. overwind incorporates the stack rectifier within the same housing. The output of the e.h.t. is 17KV and is connected to the picture tube via a special high voltage clip on cable.

Pins 6 and 7 of the transformer have the winding to supply the other picture tube supplies. Using half wave rectification D10 produces approx. 800V which is used as the DC bias for the dynamic focusing. D11 provides the negative voltage for the control grid of the picture tube (brightness control). C34 is the filter capacitor for the negative voltage supply. A larger than usual filter capacitor is used for this supply so that it will retain bias on the grid for a long period after switch-off to avoid spot burn.

Power for the picture tube heater is obtained from pins 1 and 2 on the horizontal output transformer. R49 is used to trim the heater voltage to approximately 6.3V RMS.

The transformer also generates the h.t. line voltage for the video output stage. This is obtained from pins 3 and 5 with D9 and C58 being the rectifier and filter.

All these supplies are connected to the CRT P.C.B. (VDU02) via the 9 way notched flat ribbon cable.

9.2.8 DYNAMICS FOCUS

Geometry of the picture tube causes the scanning electron beam to travel a greater distance when deflected to a corner as compared to the distance travelled by the beam at the centre of the picture tube screen. Because of these various distances optimum focus can only be achieved at one point. In practice, using a fixed D.C. focus voltage, a comprised focus adjustment has to be made. This is usually done by optimizing focus at some point half way between a corner and the centre of the screen. The VDU01 Card, however utilizes a system known as Dynamic Focus. This system overcomes these limitations in the horizontal axis.

Dynamic Focus requires the focus voltage to be modulated at the horizontal frequency. The voltage varies depending on the position of the beam as it travels horizontally across the screen.

Tx3 is the Dynamic Focus transformer. Its primary is connected in series with the horizontal deflection coils. As the scanning current flows through the primary, the secondary produces a sine wave voltage at the horizontal frequency. This frequency is determined by C59 and the secondary inductance. The output of the secondary is capacitively coupled via C31 to the adjustable D.C. focus voltage from VR9. Mixed AC + DC voltage is connected to the picture tube focus grid via R24 on the VDU02 P.C.B.

9.2.9 VERTICAL TIMEBASE

The IC U2, is used to generate the required current for the field deflection coils. This device incorporates the functions of vertical oscillator, driver and output stage in one envelope. A class B output stage with flyback boost is used. The deflection coils are current driven; hence variation in their resistance does not affect the scan amplitude.

To obtain an optimum valve of current feedback, the sampling resistor is formed by two resistors R58 and R59 connected in parallel. The sync pulse is coupled capacitively to pin 5 and the associated 2.2k ohm resistor reduces the impedance of the feeding line to a level at which pick up of horizontal pulses is of little significance.

To ensure good tracking between horizontal and vertical scans with beam current variations, the height control is fed from the 24V DC line filered by R69 & C44.

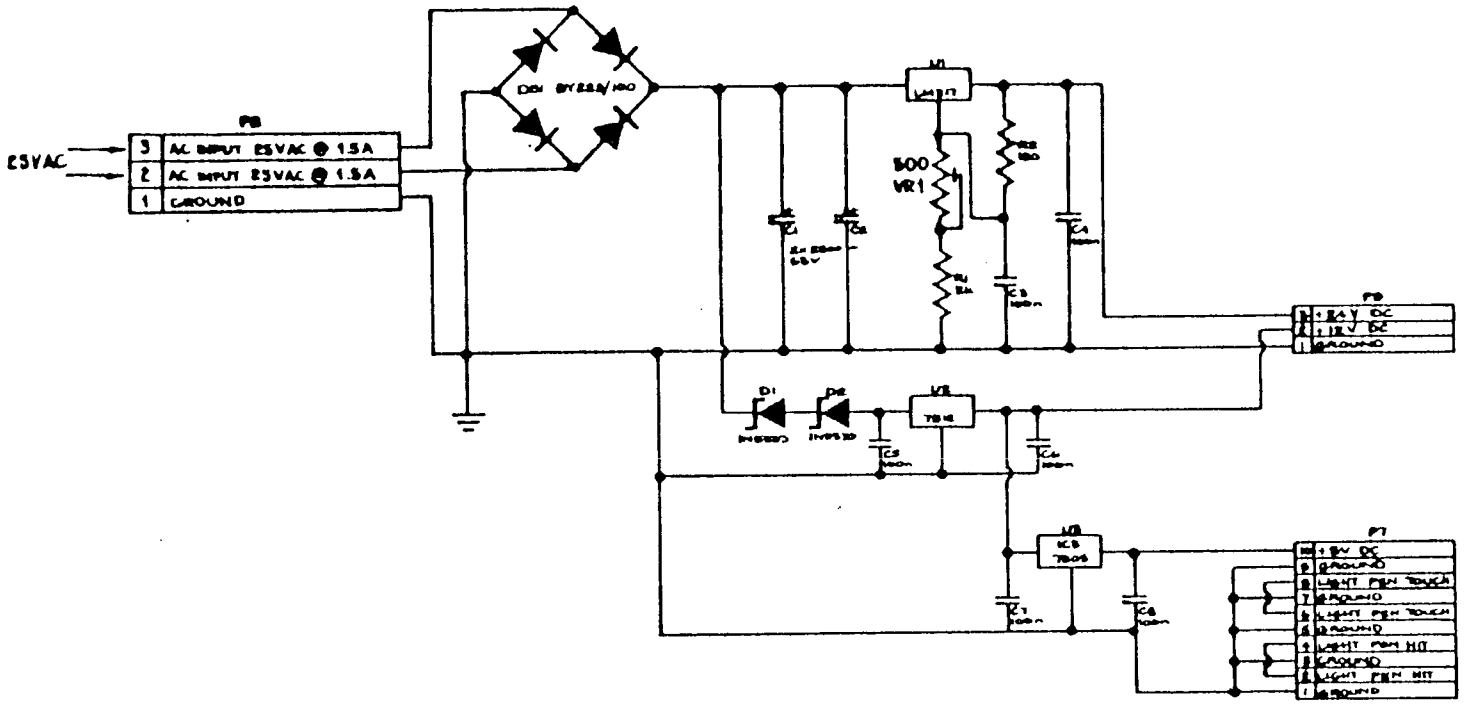
## 10. CRT CARD VDU02.

### 10.1 Circuit description.

10.1.1 Video Output Stage.

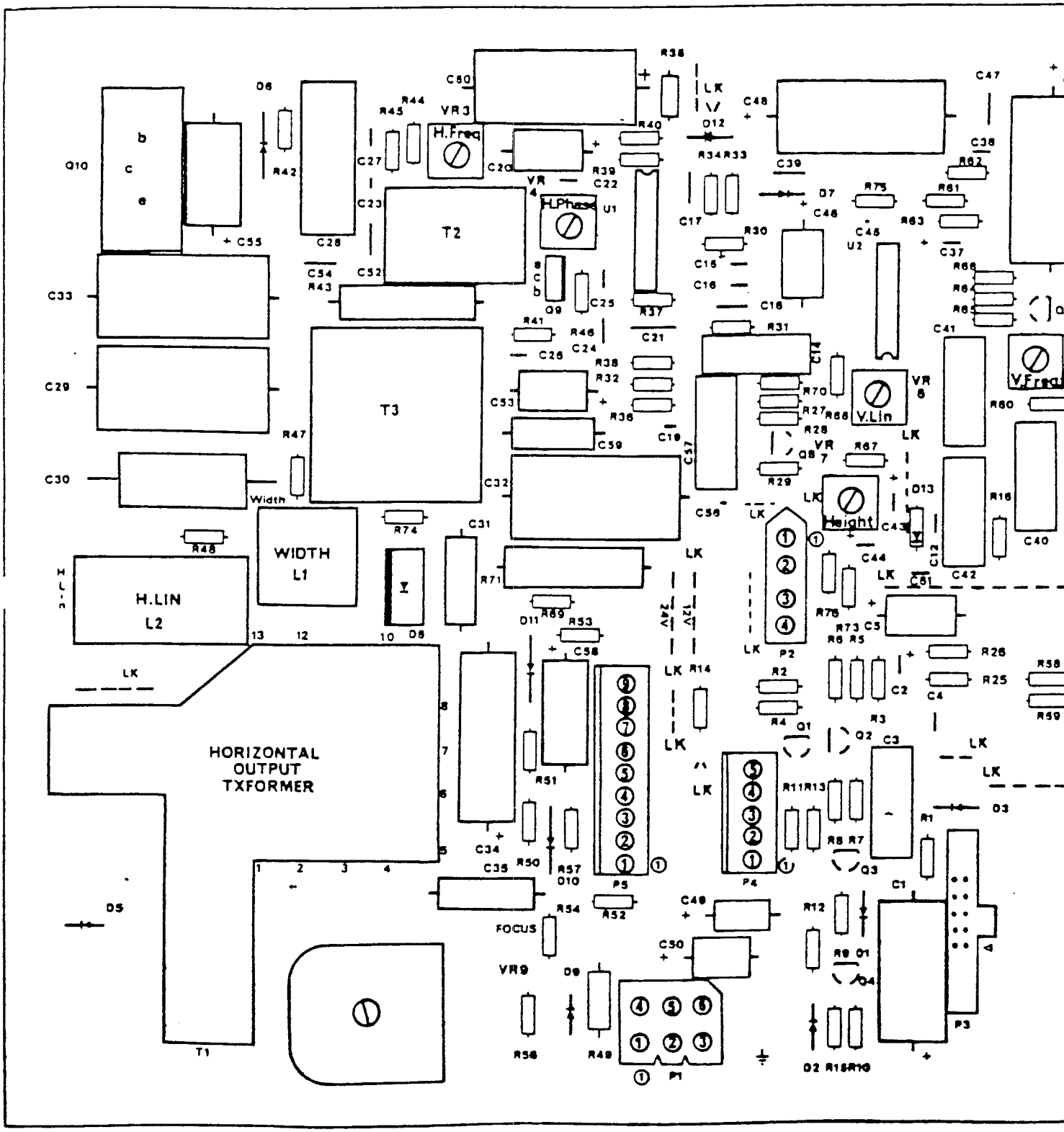
The output circuit consists of the emitter-driven video transistor Q6 and the collector load resistor R20. A zener diode D4 andits associated components hold the base of the video transistor at a d.c. potential of 7.5V.

The emitter of this transistor driven by Q7, is a high frequency transistor. The overall voltage gain of this stage is 17.

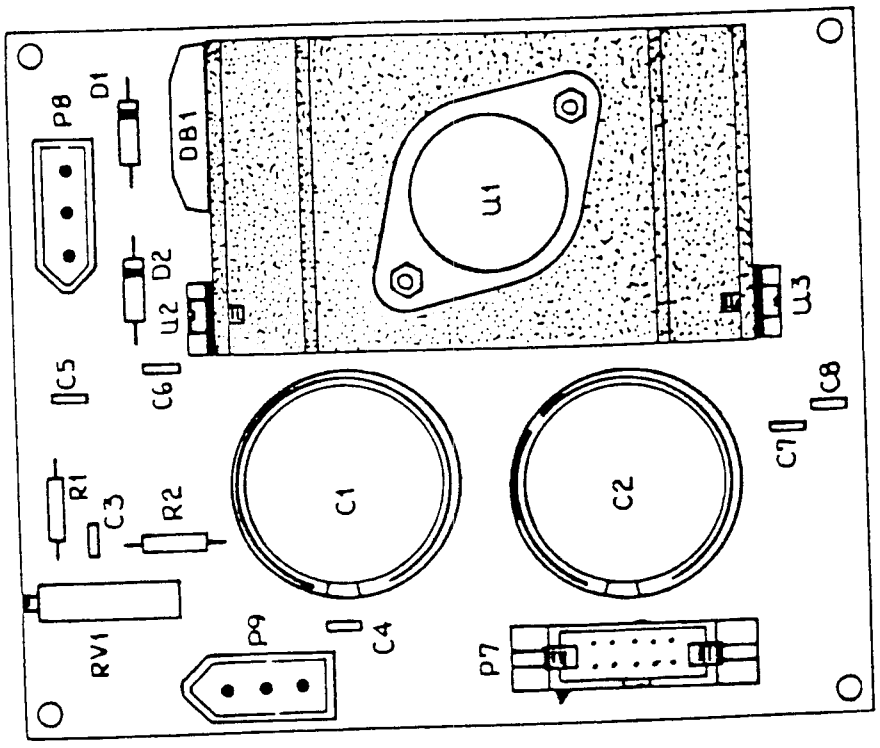



POWER SUPPLY CARD VDU03

| ITEM | DESCRIPTION | REQ'D | MATERIAL | REMARKS |
|---|---|---|---|---|
| | POWER SUPPLY CARD VDU03 | SCALE | | PASSED / DATE |
| | | — | | — / 14/7/81 |
| | SHEET 1 of 1 | DRAWN | JRL | DRAWING NUMBER |
| | FAIRLIGHT INSTRUMENTS 15 BOUNDARY ST RUSHCUTTERS BAY NSW AUSTRALIA 2011 | TRACED | | VDU 03-01 |
| | | CHECKED | C.T. | |

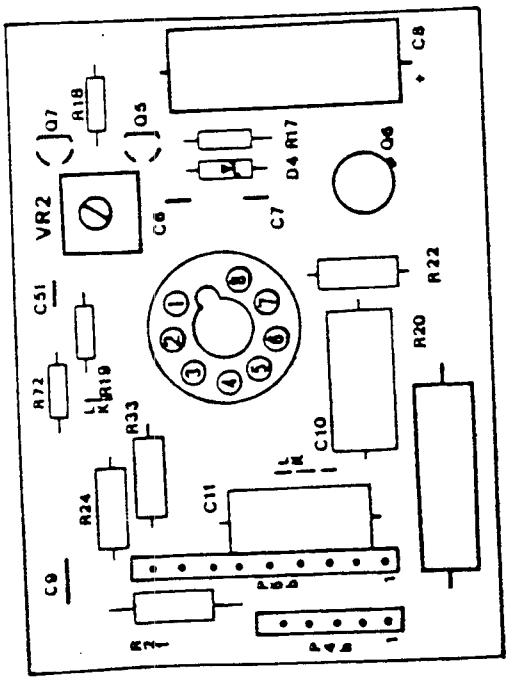



MAIN CIRCUIT CARD VDU 01




VDU03

VDU POWER SUPPLY CARD




CRT CARD VDU03

# 13.ELECTRICAL PARTS LIST.

## 13.1 Parts List for Main Card VDU01

| Circuit Ref. | Part No. | Description |
|---|---|---|
| | **TRANSISTORS** | |
| Q1 | D3011 | BC549 |
| Q2 | D3016 | BC559 |
| Q3 | D3016 | BC559 |
| Q4 | D3011 | BC549 |
| Q8 | D3016 | BC559 |
| Q9 | D4001 | BD131 |
| Q10 | D4005 | BU426 |
| Q11 | D3011 | BC549 |
| | **INTEGATED CIRCUITS** | |
| U1 | B0049 | TDA2591 |
| U2 | B0048 | TDA2651 |
| | **DIODES** | |
| D1 | D5014 | BAW62 |
| D2 | D5014 | BAW62 |
| D3 | D5014 | BAW62 |
| D5 | D5017 | BYV96E |
| D6 | D5016 | BYW96E |
| D7 | D5013 | BAS11 |
| D8 | D5018 | BY229/400 |
| D9 | D5017 | BYV96E |
| D10 | D5015 | BY184 |
| D11 | D5015 | BY184 |
| D12 | D5008 | IN4004 |
| D13 | D5009 | IN914 |

## RESISTORS

All resistors are 1/4w, +-5% Metal Film Type unless otherwise indicated. Values in ohms.

| Circuit Ref. | Part No. | Description. |
|---|---|---|
| R1 | R1012 | 82 |
| R2 | R1040 | 18K |
| R3 | R1033 | 4K7 |
| R4 | R1013 | 100 |
| R5 | R1013 | 100 |
| R6 | R1021 | 470 |
| R7 | R1049 | 100K |
| R8 | R1025 | 1K |
| R9 | R1037 | 10K |
| R10 | R1029 | 2K2 |
| R11 | R1045 | 47K |
| R12 | R1040 | 18K |
| R13 | R1011 | 68 |
| R14 | R1009 | 47 |
| R15 | R1047 | 68K |
| R16 | R1033 | 4K7 |
| R25 | R1022 | 560 |
| R26 | R1067 | 3M3 |
| R27 | R1064 | 1M8 |
| R28 | R1031 | 3K3 |
| R30 | R1026 | 1K2 |
| R31 | R1031 | 3K3 |
| R32 | R1065 | 2M2 |
| R33 | R1038 | 12K 2% |
| R34 | R1048 | 82K |
| R35 | R1050 | 120K |
| R36 | R1043 | 33K |
| R37 | R1017 | 220 |
| R38 | R1017 | 220 |
| R39 | R1002 | 12 |
| R40 | R1001 | 10 |
| R41 | R1014 | 120 |
| R42 | R1048 | 82K |
| R43 | R5006 | 68 5 WATT |
| R44 | R1076 | 1R8 |
| R45 | R1011 | 68 |
| R46 | R1017 | 220 |
| R47 | R1028 | 1K8 |
| R48 | R1028 | 1K8 |
| R49 | R4006 | 10 1 WATT |

| Circuit Ref. | Part No. | Description. |
|---|---|---|
| R50 | R1028 | 1K8 |
| R51 | R1025 | 1K |
| R52 | R2002 | 1M Carbon Film 1/2 WATT |
| R53 | R1065 | 2M2 |
| R54 | R2003 | 1M5 Carbon Film 1/2 WATT |
| R56 | R2003 | 1M5 Carbon Film 1/2 WATT |
| R57 | R1064 | 1M8 |
| R58 | R1076 | 1R8 |
| R59 | R1078 | 1R5 |
| R60 | R1045 | 47K |
| R61 | R1050 | 120K |
| R62 | R1042 | 27K |
| R63 | R1029 | 2K2 |
| R64 | R1052 | 180K |
| R65 | R1051 | 150K |
| R66 | R1048 | 82K |
| R67 | R1048 | 82K |
| R68 | R1038 | 12K |
| R69 | R1025 | 1K |
| R70 | R4013 | 15 1 WATT |
| R71 | R5007 | 2R2 5 WATT |
| R72 | R1008 | 39 |
| R73 | R1018 | 270 |
| R74 | R1011 | 68 |
| R75 | R1055 | 330K |
| R76 | R1031 | 3K3 |
| R77 | R1013 | 100 |

VARIABLE RESISTORS

| | | |
|---|---|---|
| VR1 | R6111 | 500 Contrast |
| VR3 | R6112 | 50K Cermet Trim |
| VR4 | R6112 | 50K Cermet Trim |
| VR5 | R6113 | 100K Cermet Trim |
| VR6 | R6114 | 10K Cermet Trim |
| VR7 | R6114 | 10K Cermet Trim |
| VR8 | R6110 | 1M Brightness |
| VR9 | R6129 | 2M7 Focus |

| Circuit Ref. | Part No. | Description. |
|---|---|---|
| | | **CAPACITORS** |
| C1 | C7106 | 470u 25v Electrolytic |
| C2 | C6002 | 4u7 16v Tantalum |
| C3 | C8017 | 470n 100v Polyester |
| C4 | C2533 | 10n 100v Polyester |
| C5 | C7109 | 100u 25v Electrolytic |
| C12 | C8004 | 4n7 100v Polyester |
| C13 | C7113 | 150u 16v Electrolytic |
| C14 | C8016 | 680u 100v Polyester |
| C15 | C6005 | 22u 16v Tantalum |
| C16 | C2533 | 10n 100v Polyester |
| C17 | C2502 | 4n7 100v Silvered Mica 2% |
| C18 | C8014 | 100n 100v Polyester |
| C19 | C8007 | 6n8 100v Polyester |
| C20 | C7109 | 100u 25v Electrolytic |
| C21 | C8018 | 220n 100v Polyester |
| C22 | C2507 | 270p 50v Ceramic |
| C23 | C2542 | 82p 50v Ceramic |
| C24 | C8014 | 100n 100v Polyester |
| C25 | C2503 | 1n 50v Polyester |
| C26 | C8019 | 47n 100v Polyester |
| C27 | C2503 | 1n 50v Ceramic |
| C28 | C4005 | 12n 1KV Polypropylene |
| C29 | C4003 | 1u 400v Polycarbonate |
| C30 | | selected if needed |
| C31 | C4002 | 1n 1KV Polycarbonate |
| C32 | C4003 | 1u 400v Polycarbonate |
| C33 | C4003 | 1u 400v Polycarbonate |
| C34 | C7125 | 10u 200v Electrolytic |
| C35 | C4004 | 10n 1KV Polycarbonate |
| C36 | C7104 | 1000u 25v Electrolytic |
| C37 | C6001 | 1u 35v Tantalum |
| C38 | C2531 | 330p 50v Ceramic |
| C39 | C8014 | 100n 100v Polyester |
| C40 | C8017 | 470n 100v Polyester |
| C41 | C8017 | 470n 100v Polyester |
| C42 | C8017 | 470n 100v Polyester |
| C43 | C6005 | 22u 16v Tantalum |
| C44 | C6005 | 22u 16v Tantalum |

| | | | | |
|---|---|---|---|---|
| C45 | C2505 | 100p | 50v | Ceramic |
| C46 | C7109 | 100u | 25v | Electrolytic |
| C47 | C8014 | 100n | 100v | Polyester |
| C48 | C7106 | 470u | 25v | Electrolytic |
| C49 | C7108 | 100u | 40v | Electrolytic |
| C50 | C7109 | 100u | 25v | Electrolytic |
| C52 | C8014 | 100n | 100v | Polyester |
| C53 | C7107 | 47u | 25v | Electrolytic |
| C54 | C8014 | 100n | 100v | Polyester |
| C55 | C7108 | 100U | 40V | Electrolytic |
| C56 | C2505 | 100p | 50 | Ceramic |
| C57 | C8017 | 470n | 100v | Polyester |
| C58 | C7126 | 2u5 | 200v | Electrolytic |
| C59 | C4002 | 1n | 1k | Polycarbonate |
| C60 | C7120 | 470u | 16v | Electrolytic |
| C61 | C2543 | 220n | | Ceramic Disc |

## TRANSFORMERS

| | | |
|---|---|---|
| TX1 | G5196 | HORIZONTAL OUTPUT |
| TX2 | G5195 | HORIZONTAL DRIVER |
| TX3 | G5192 | DYNAMIC FOCUS |

## COILS

| | | |
|---|---|---|
| L1 | G5197 | WIDTH |
| L2 | G5194 | LINEARITY |
| L3 | G5184 | DEFLECTION YOKE |

## MISCELLANEOUS

| | | |
|---|---|---|
| P1 | G5211 | 6 PIN CONNECTOR |
| P2 | G5242 | 4 PIN CONNECTOR |
| P3 | D6003 | 10 PIN CONNECTOR |
| P4 | G5246 | 5 PIN CONNECTOR |
| P5 | G5244 | 9 PIN CONNECTOR |
| - | G6017 | EHT Cable and Cap |

13.2 Parts List for CRT Card VDU01

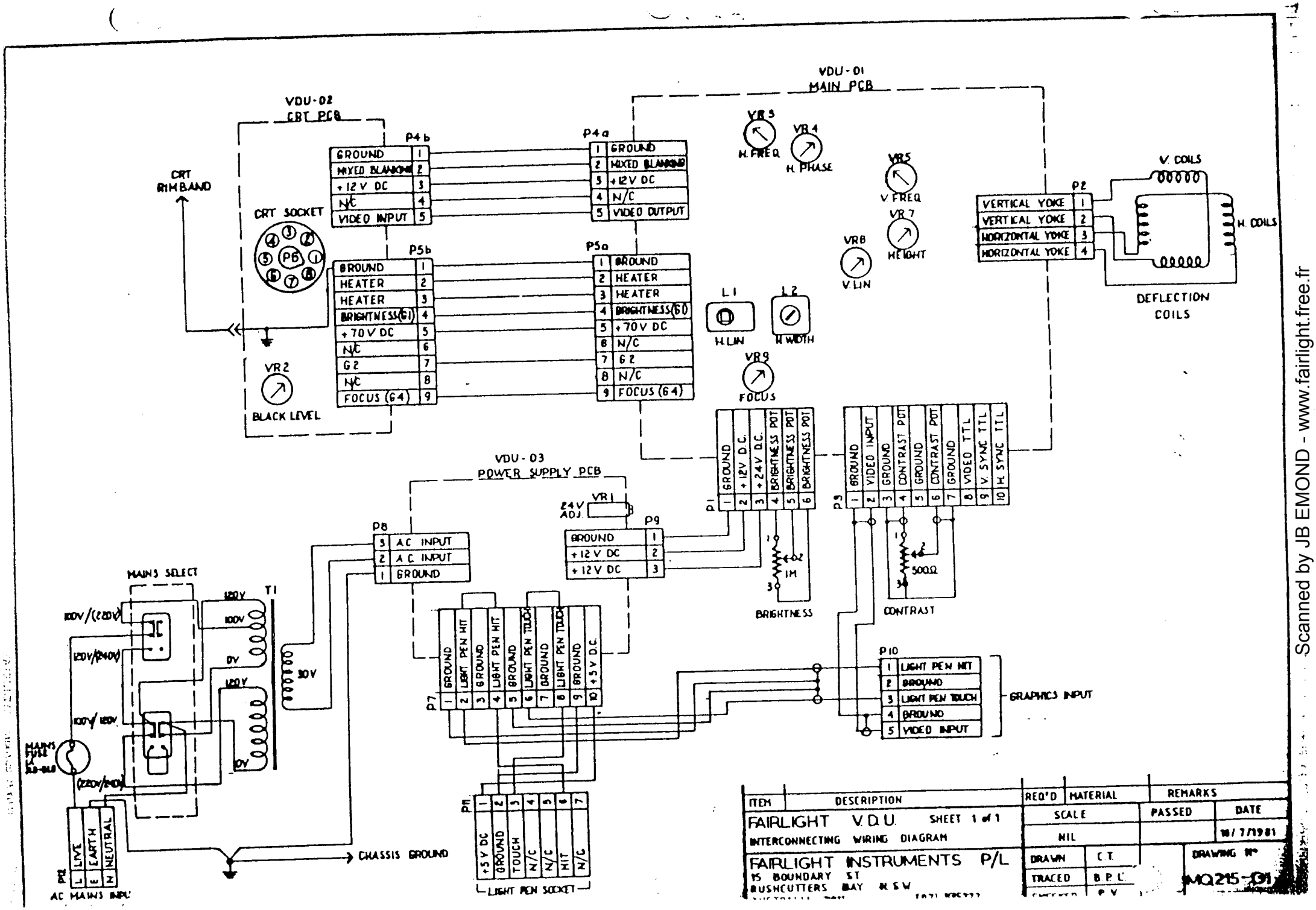
| Circuit Ref. | Part No. | Description | |
|---|---|---|---|
| | | **TRANSISTORS** | |
| Q5 | D3011 | BC549 | |
| Q6 | D4002 | BF337 | |
| Q7 | D3021 | BSX20 | |
| | | **DIODES** | |
| D4 | D5012 | BZY88/7V5 | ZENER |
| | | **RESISTORS** | |

All resistors are 1/4w, +- 5% Metal Filmtype unless other-wise indicated. Values in ohms.

| | | | |
|---|---|---|---|
| R17 | R1023 | 680 | |
| R18 | R1023 | 680 | |
| R19 | R1010 | 56 | |
| R20 | R5005 | 1K2 | 5 Watt |
| R21 | R1009 | 47 | |
| R22 | R2005 | 470 | Carbon Film |
| R23 | R2000 | 22k | Carbon Film |
| R24 | R2001 | 220K | Carbon Film |
| VR2 | R6117 | 1K | Cermet Trim |
| | | **CAPACITORS** | |
| C6 | C2533 | 10N 50v | Ceramic |
| C7 | C2533 | 10n 50v | Ceramic |
| C8 | C7124 | 20u 100v | Electrolytic |
| C9 | C2525 | 100n 50v | Ceramic |
| C10 | C4001 | 100n 400v | Polycarbonate |
| C11 | C4004 | 10n 1KV | Polycarbonate |
| | | **MISCELLANEOUS** | |
| P6 | G5193 | 8 PIN CRT Socket | |

13.3 Parts List For Power Supply Card VDU03

| Circuit Ref. | Part No. | Description. |
|---|---|---|
| | **IC'S** | |
| U1 | D1006 | LM317 |
| U2 | D0812 | 7812 |
| U3 | D0805 | 7805 |
| | **DIODES** | |
| D1 | D5004 | IN5339 ZENER |
| D2 | D5004 | IN5339 ZENER |
| DB1 | D2010 | BY225 BRIDGE RECTIFIER |
| | **RESISTORS** | |
| R1 | R1079 | 2K 1/4 Watt |
| R2 | R1013 | 120 1/4 Watt |
| VR1 | R6204 | 500R Multi Turn Pot |
| | **CAPACITORS** | |
| C1 | C7129 | 2500 <63v Electrolytic |
| C2 | C7129 | 2500u 63v Electrolytic |
| C3 | C1010 | 100n 100v Ceramic |
| C4 | C1010 | 100n 100v Ceramic |
| C5 | C1010 | 100n 100v Ceramic |
| C6 | C1010 | 100n 100v Ceramic |
| C7 | C1010 | 100n 100v Ceramic |
| C8 | C1010 | |



## 16. MECHANICAL PARTS LIST.

### 16.1 Parts List for Exploded View MQ2151/01.

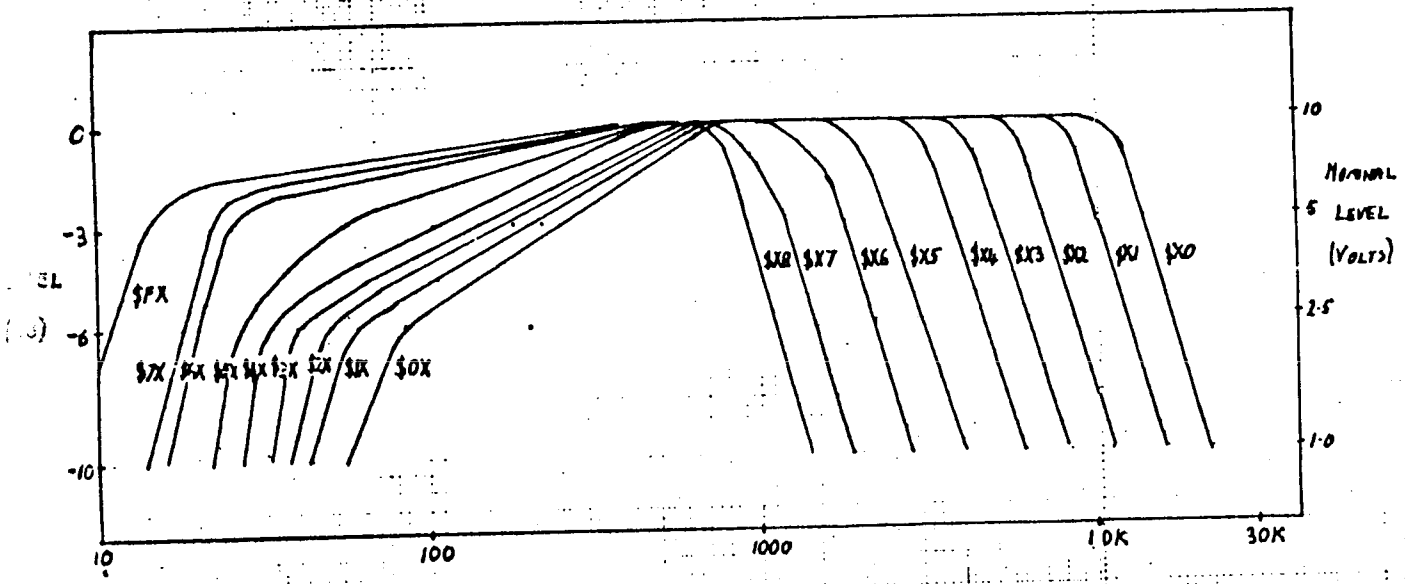
| Ref No. | Part No. | Description. |
|---|---|---|
| 1 | G5152 | Light Pen Socket |
| 2 | G5151 | Light Pen |
| 3 | J0209 | Front Panel Assy. |
| 4 | J0208 | Base Panel |
| 5 | G5191 | Power Transformer |
| 6 | G0073 | Power Supply Base Plate |
| 7 | G5159 | Voltage Selector Switch |
| 8 | J0040 | Rear Panel Escutcheon |
| 9 | G5190 | Fuse Holder Cap |
| 10 | G5309 | Fuse Holder |
| 11 | D6768 | Power Connector 3 pin |
| 12 | D6710 | Graphics Connector 5 pin |
| 13 | G0128 | P.C.B. Bracket |
| 14 | G0127 | Support strip |
| 15 | G0124 | Support Panel LH |
| 16 | G0126 | Support bracket |
| 17 | G0125 | Support Panel RH |
| 18 | MVDU02 | CRT Card VDU02 |
| 19 | MVDU01 | Main Card VDU01 |
| 20 | G5184 | Deflection Yoke |
| 21 | G5198 | Picture Tube 15" |
| 22 | G6017 | eht cable |
| 23 | MVDU03 | P.S.U. Card VDU03 |
| 24 | R6111 | Contrast Pot |
| 25 | R6110 | Brightness Pot |
| 26 | G5107 | P.C.B. Standoff |
| 27 | H0125 | Screw 6Gx1/4" |
| 28 | H0102 | Screw CHD4BAx" |
| 29 | H0111 | Screw CKS 4BAx15/16" |
| 30 | H0118 | Screw CKS6BAx3/8" |
| 31 | H0115 | Screw 4Gx3/8" |
| 32 | H0140 | Stud 1/4"W |
| 33 | H0133 | Screw CHD 4BAx1/4" |
| 34 | H0008 | Washer 4BA star |
| 35 | H0021 | Washer Pot |
| 36 | H0139 | Washer 1/4"W Star |
| 37 | H0012 | Washer 6BA Star |
| 38 | H0202 | Nut 4BA Hex |
| 39 | H0208 | Nut Fuseholder |
| 40 | H0201 | Nut 6BA Hex |
| 41 | H0020 | Nut Pot |

16.2 Parts List for Exploded View MQ2151/02.

| Ref.No. | Part No. | Description. |
|---|---|---|
| 1 | J0209 | Front Panel |
| 2 | J0271 | Top Cover |
| 3 | J0208 | Base Panel |
| 4 | J0006 | Foot |
| 5 | H0132 | Screw 1/4"x1" |
| 6 | H0103 | Screw 8Gx3/4" CHD |
| 8 | H0209 | Nut |

# APPENDIX

## MASTER CARD BANDPASS FILTER CHARACTERISTICS.




NOTE: $NN means hexadecimal notation for filter setting
X means "don't care"