ADC Direct Input
  Connector type: Cannon XLR 3 pin
  Input signal: D.C. coupled
  Sensitivity: 10 volts p-p for full scale conversion
  Impedance: 100K ohms

3.3 DIGITAL

Processor: Dual 6809

Memory: 256K bytes Program RAM
        128K bytes Waveform RAM
        16K bytes Video RAM

Floppy Disk: 2 x Mitsubishi M2896-63
             8 inch double sided, single/double density
             Soft sectored, 128/256 bytes per sector

Graphics Display: Bit mapped VRAM
                  Composite video output
                  1 volt p-p nominal
                  75 ohms impedance

Input/Output: Serial RS232C, 9600 Baud

3.4 MECHANICAL

Dimensions: Width 750 mm
            Depth 450 mm
            Height 320 mm

Weight: 40 kilograms

HH;F	Fill memory from beginning address to end address
BEG ADDR	User prompt for beginning address
END ADDR	User prompt for end address
<CTRL X>	Abort current command line, take no action
<	Close current location, return to sequence start and open
AAAA,R	Relocate address AAAA by register R. R may be any of the CPU registers, the user relocation register, the monitor flag byte or the currently open location
AAAA.	Relocate address AAAA by Relocation Register $R
:	Same as linefeed (CTRL J) except that no new line is taken, and neither the address nor contents of the next location is displayed
AAAA#LL	Memory dump of LL lines (16 bytes/line) starting from address AAAA
'<ASCII chr>	Input ASCII character value instead of hex value for any of the above commands

The 6809 monitor will also accept input of signed hex numbers.

4.2.1.4 System Boot/Disk ROM

This ROM is used by CPU#2 for disk booting operations and occupies locations F800 to FBFF in the unique ROM space for CPU#2.

The following functions calls are provided:-

* Boot load QDOS operating system from disk
* Initialise disk controller
* Read full last sector
* Read partial last sector
* Read verify (CRC check only)
* Write and verify CRC
* Restore head (seek track 0)
* Seek to specified track
* Write test
* Write D.D. mark to sector
* Write sectors and verify CRC
* Write sectors and don't verify CRC
* Check and abort if non-recoverable error

This ROM contains the code to load the actual disk drivers into system RAM. The driver routines themselves are stored in RAM after being loaded from the ROM on the QFC9 floppy controller card, and the Q077/Q087 Hard Disk card if present.

4.4 QFC9 FLOPPY DISK CONTROLLER FUNCTIONAL DESCRIPTION

4.4.1 INTRODUCTION

The floppy interface card interfaces the bit parallel/serial buss of floppy disk drives to the C.M.I.'s interleaved parallel buss. The interface is a combination of device driver software, controlling disk data format and initialization of data transfer parameters, and the hardware which carries out the transfers without processor intervention.
Data is stored on the floppy disk itself on its magnetic coating, in concentric rings. In a standard, 8 inch floppy there are 77 such rings on each side called tracks. Tracks are divided into data blocks called sectors. Sectors in Fairlight disk formats are either 128 or 256 bytes per sector, depending on operating system being used. The smallest amount of data that can be read to or from a disk is one sector. Sectors on a disk may be randomly accessed.

Track 0 is outermost. The controller automatically restores to this track on power on, and on reaching track 0, signals the controller by a mechanical switch generated signal. All head movement is relative to this reset state.

Floppy drives transfer data serially. They also have parallel control lines to control drive number selection, head stepping direction, head load, disk write and disk write enable. The head of the drive must be lowered to the disk surface before a transfer may take place, this is operation referred to as "head load". Index pulses are generated by the drive so that the controller knows the location of the rotating disk. This pulse occurs once per revolution, so the start of tracks can be determined by the controller. Also, the controller generates pulses that are used to step the head in and out to position it over the required track.

The Floppy Disk Controller/Formatter uses the WD1791 controller LSI. It is software selectable to double density, double sided in addition to single density, single sided. It is designed to work with CPU #2's, transferring data to and from memory by DMA on Processor 2. The processor is not involved with transferring data to and from the disk. Once a data transfer is set up the processor may continue processing other tasks until the interrupt for "command complete" is issued by the controller.

4.4.1.1 Address Map
(refer to drawing QFC9-01)

The controller is accessed through two locations, in a memory map which enables access to peripherals. An address register is set up to point to the required controller register. All data is read or written through a single data register.

ADDRESS (HEX)	READ	WRITE
FCE0	data	data
FCE1	status register	address register

The 7 controller registers are ...

00 control register
02 DMA address (low byte)
04 DMA address (high byte)
06 byte count to read/write (low byte, inverted)
08 byte count to read/write (high byte, inverted)
0A command location to load device driver ROM into RAM
WD1791 L.S.I
0C cmd (write) status(read)
0D track r/w
0E sector r/w
0F data r/w

The definitions of the control register bits are ...

0 DS0 drive select address bit 0
1 DS1 drive select address bit 1
2 enable interrupt (active high)
3 enable DMA address incrementing (active low)
4 DMA transfer direction(1= to disk)
5 side select
6 retrig head load timer
7 DENS density selection

The definitions of the control status bits are ...

0 0 always zero
1 n/c
2 n/c
3 ready
4 two sided
5 disk change
6 interrupt
7 device driver loading (active low)

4.4.1.2 Commands

The extensive instruction set of the 1791 LSI can be obtained from the manufacturers data sheets for the 1791. This device handles all data conversions between the disk drive and the C.M.I. buss.

4.4.2 DATA BUFFERS, DMA ADDRESS COUNTER
(refer to drawing QFC9-02)

4.4.2.1 DMA address Counters

Sixteen bit counter chain C1 to C4 is used to provide the address for DMA transfers. The starting address for each disk transfer is established by writing the appropriate byte address to the address register then writing the address byte to the data register and then repeating for the other address byte. This causes the address to be preset into the DMA address counters by means of parallel-load strobe pulses STAL (low byte) and STAH (high byte). The incrementing of the DMA counters may be inhibited under software control, so that disk data may be dumped directly into the data portholes on channel cards.

4.4.2.2 DMA byte transfer counters
(refer to drawing QFC9-04)

Sixteen bit counter chain C5 to C8 is used to transfer the required number of bytes to or from disk. It must be initialized with the inverse of the number of bytes to be transfered. Any number may be specified up to a maximum of 65,535 bytes. Only those bytes specified will be transfered to memory on a disk read. This allows less than a sector to be read from disk, and saves the software overhead required to handle partial sector reads. The read takes place but the buss VMA signal goes inactive after the required number of bytes have been transfered, so disabling memory writes. The VMA disable signal is generated from the ripple carry out on this counter chain, by buffering /FINPS, (Finished Partial Sector).

When a transfer occurs, the DMAC (Direct Memory Access Claim) line is generated so that the memory card swaps maps, allowing data to be dumped into memory currently not mapped into the processor's address space. This signal is generated by the components around flip-flop A11.

4.4.2.3 Data Buffers
(refer to drawing QFC9-02)

Data is propagated from the system data bus via latch B6 which holds the data across the processor 1 phase. This latched data also becomes the DATA FROM BUS via buffer B5, to the floppy-controller LSI.

Data written to the system control register at 00 is latched by B7. This controls such functions as drive select and DMA direction.

4.4.3 ADDRESS DECODING, CONTROLLER LSI

4.4.3.1 Address Decoding

Address range $FCE0-$FCE1 is decoded by gates B1, E1, B2, E1 and latched by D2.

Address $FCE0 is used to enable the internal data buss to read and write to controller functions.
Address $FCE1 data is latched by B8 and with the access to FCE0 generates the internal chip selects and read/write strobes through C9.

Inverting buffer E5 and open collector drivers E6, E7 are used to interface the 1791 LSI controller to the disk drive cable. Incoming disk status signals are pulled up by 150 ohm terminating resistors.

4.4.3.2 Controller L.S.I.

The Interrupt Request from the LSI is gated with the Interrupt Enable to provide an open-collector interrupt signal for the system IRQ on buss pin 63A.

4.4.4 DMA LOGIC
(refer to drawing QFC9-03)

Data requests from the 1791 or Device Driver ROM loading are synchronised with Processor 2 Phase 2 using flip-flops C1 and A10. This sets up a DMA request to the processor (RDMA). DMA cycles are granted by ACK acknowledge signal.

Flip-flop A11 only allows a DMA cycle to occur every second Processor cycle (the floppy drive can not transfer at that rate but this is a system constraint on other DMA devices in the DMA daisy chain).

The DMA daisy chain is controled by /ENL and /EDL. Respectively these stand for, Enable Next Level and Enable DMA Level. When /EDL is active, a DMA request may be requested by the highest priority device. The /ENL signal informs the next device in the daisy chain that it may make a request if higher priority devices have not.
Depending on which function has been requested (Reset, Read, write) the required DTB (Data to Bus), and ATB (Address to Bus) signals are issued.

4.4.5 CONTROL REGISTER

The control register contains the drive number select bits, density selection, interrupt enable, increment DMA address enable, data transfer direction, side select and retrigger head load delay. This register is the latch at B7. The "retrig head" signal is used to reactivate the head load delay when the drive number has been changed, to allow for head bounce.

4.4.6 MASTER OSCILLATOR
(refer to drawing QFC9-05)

The LSIs used on the card require a master 16MHz clock. This is generated with the components around the 74S04 at F5. The FDC9229 generates the 2 Mhz clock for the 1791, by dividing this internally.

4.4.7 WRITE PRECOMPENSATION

In double density operation there may be a time shift applied to the data when it is being written to the inner disk tracks (>45). The amount of shift is determined by the LSI and the floppy disk suport device 9229. They produce a programmable delay of 1 to 3 clock cycles.

The amount, if any, is specified by the drive manufacturer. Links W4, W5, W6, W7 select the amount. The amount on inner and outer tracks can be independently set.

W5	W6	W7	Precompensation Value (in nS)
0	0	0	0
0	0	1	62.5
0	1	0	125
0	1	1	187.5
1	0	0	250
1	0	1	250
1	1	0	312.5
1	1	1	312.5

The precompensation value is normally set to 0 on inner and outer tracks. It is more important on inner tracks as the bit density on the disk is greater.

W4 selects minifloppy drives and also requires the board to be made with a 34 pin connector (or a special cable) and an 8MHz crystal.

4.4.8 DATA SEPARATOR

The serial data stream that comes from the drive is in a synchronous form. It has embedded the required data as well as clock pulses and syncronization "marker bytes".

The data separator is used to generate the data window from the FM (single density) or MFM (double density) encoded READ DATA supplied by the disk drive. The separator tracks, so that incoming data is always in the center of the data window. This data window informs the controller chip which bits in the data stream it is receiving are data and which are clock bits just used in the data encoding scheme.

The separator is a digital phase locked loop in the FDC9229 chip at E10. This chip does all the work of data separation.

4.4.9 DEVICE DRIVER ROM

The disk controller software may be placed in a 2K or 4K EPROM on the controller card. This EPROM is not in the processors directly addressable memory. It is executed by reading the software into RAM. This is done by DMA. The EPROM is copied into RAM as if reading a disk, except much faster.
The least significant DMA counter lines are used as addresses on the EPROM, so the EPROM can only be loaded into memory on 2k or 4k boundaries. The flip-flop C11 and gates in D11 and B11 produce a DMA write to memory request that is terminated after the byte counter times out.

7.12 Slot 19: Floppy Disk Controller QFC-9

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
71	EDL	Enable Daisy Links	O/P	Floppy ($\overline{ETL}$)
70	ETL	Enable This Level	I/P	Floppy ($\overline{EDL}$)
69	ENL	Enable Next Level	O/P	H.Disk ($\overline{ETL}$)
68	DMACLM	DMA claim	O/P	RAM ($\overline{DMAC21}$)
65	PENB	Peripheral Enable	I/P	RAM card 0
63	IRQD	Floppy Controller IRQ	O/P	Q133 (IL72)
48	ACK2	DMA cycle grant	I/P	Processor
47	RDMA	DMA request	O/P	Processor ($\overline{REQ2}$)

7.13 Slot 20: Hard Disk Controller Q077

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
71	EDL	Enable Daisy Links	O/P	N/C
70	ETL	Enable This Level	I/P	Floppy ($\overline{ENL}$)
69	ENL	Enable Next Level	O/P	N/C
68	DMACLM	DMA claim	O/P	RAM ($\overline{DMAC22}$)
65	PENB	Peripheral Enable	I/P	RAM card 0
63	IRQD	Hard Disk Controller IRQ	O/P	Q133 (IL72)
48	ACK2	DMA cycle grant	I/P	Processor
47	RDMA	DMA request	O/P	Processor ($\overline{REQ2}$)

9.8 DISK DRIVE REMOVE/REPLACE

9.8.1 Disk Drive removal.

1. Unscrew the rear panel as in section 9.3 but do not completely remove.
2. Disconnect the disk drive's signal and power cables.
3. Replace the rear panel to the mainframe.
4. Remove both of the mainframe side covers, top cover and bottom cover, (four counter-sunk Philips-head screws secure each mainframe cover). Refer sections to 9.5, 9.6 and 9.7.
5. Turn machine over onto its left-hand side. Refer figure 9.1.
6. Remove the four screws securing the disk drive to the mainframe, (two on the top side and two on the bottom side of the disk drive mounting plates).
7. Slowly slide out the disk drive from the mainframe. Refer figure 1.

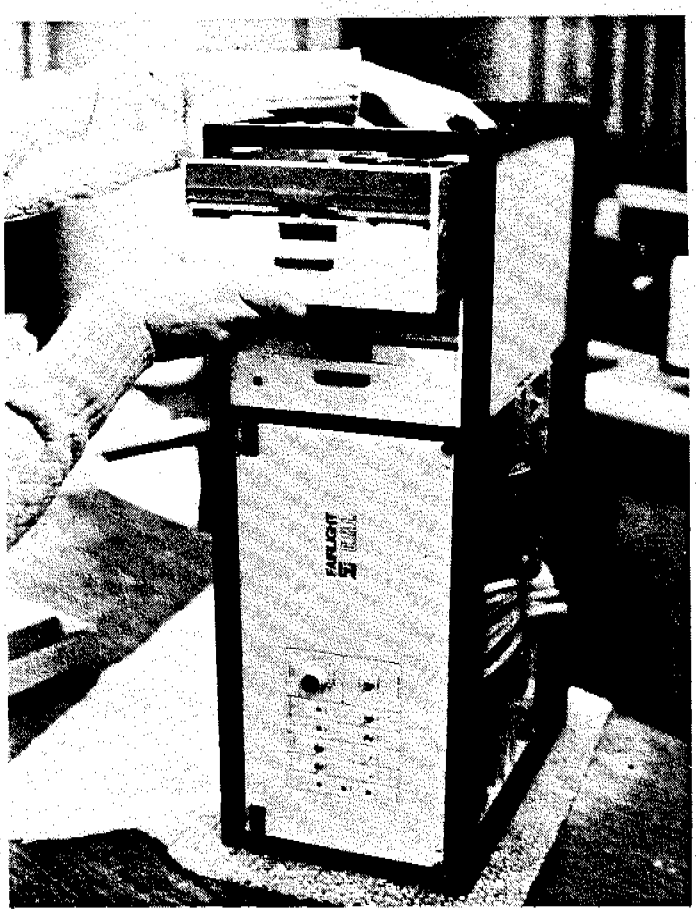


Figure 9.1 Disk Drive Removal

9.8.2 Disk drive replacement.

NOTE: Replacement disk drive should be 'optioned' and 'drive number selected' before inserting into mainframe. Refer to DISK DRIVE Manual section.

1. Once the replacement disk drive has been 'optioned' and 'drive number selected', slide the drive into the mainframe.
2. Replace the four disk drive mounting screws removed in 9.8.1.
3. Replace bottom cover and gently lower CMI back down onto its base.
4. Again remove the rear panel and reconnect the cables removed in 9.8.1. and replace rear panel.
5. Replace the two side panels and top cover.

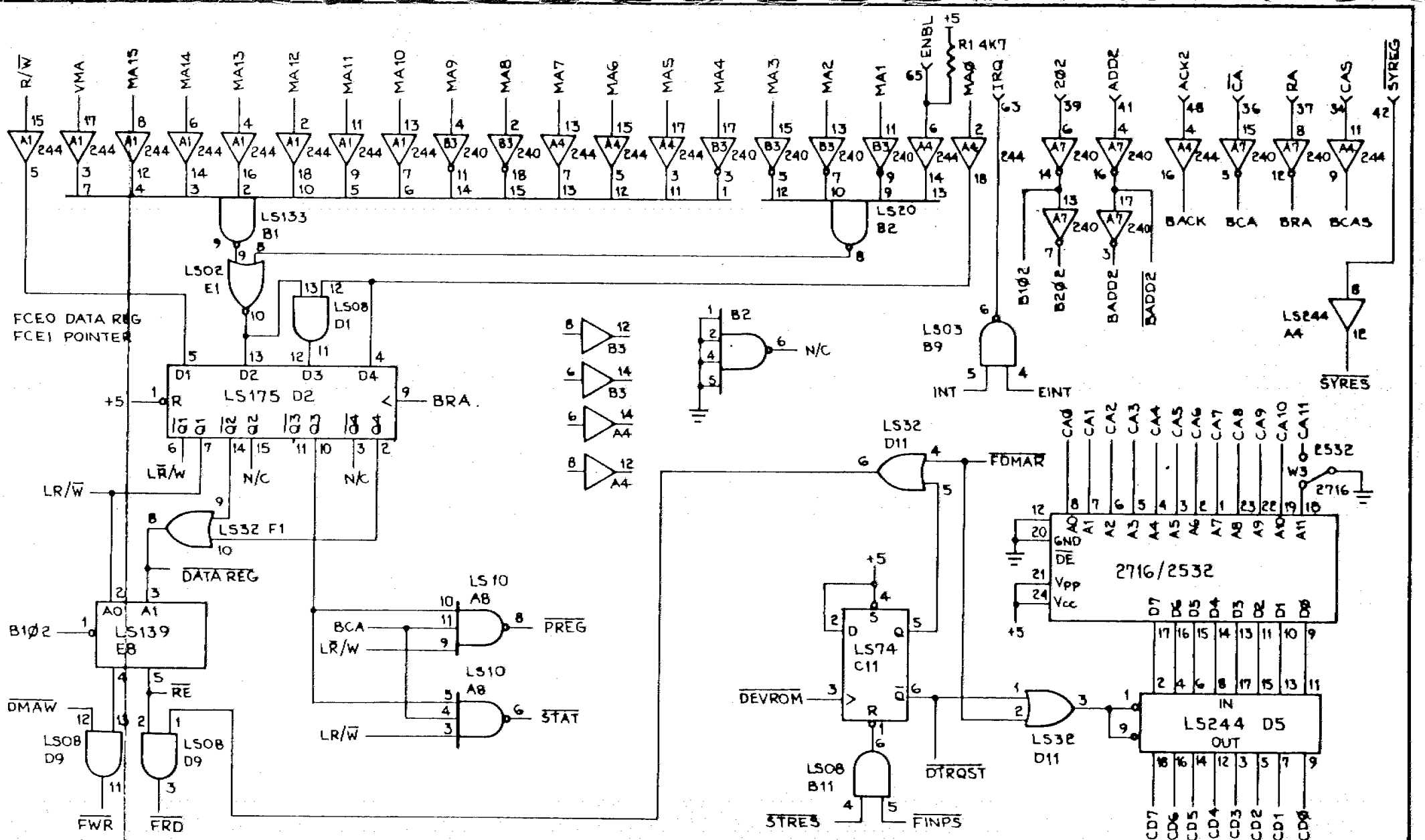
9.9 FAN ASSEMBLY REMOVE/REPLACE

1. Disconnect mains power.
2. Remove top cover, as in section 9.5.
3. Disconnect the 6-way power cable going to the Fan asssembly. A locking tab on the connector has to be depressed before the connector can be unpluged.
4. Remove the six mounting screws and washers from the top of the Fan assembly. Note that under each washer there is a steel spacer inside the rubber grommet. Care should be taken so that these spacers are not dislodged when Fan assembly is lifted off the card cage assembly.
5. Lift off Fan assembly.

9.10 CARD CAGE REMOVE/REPLACE

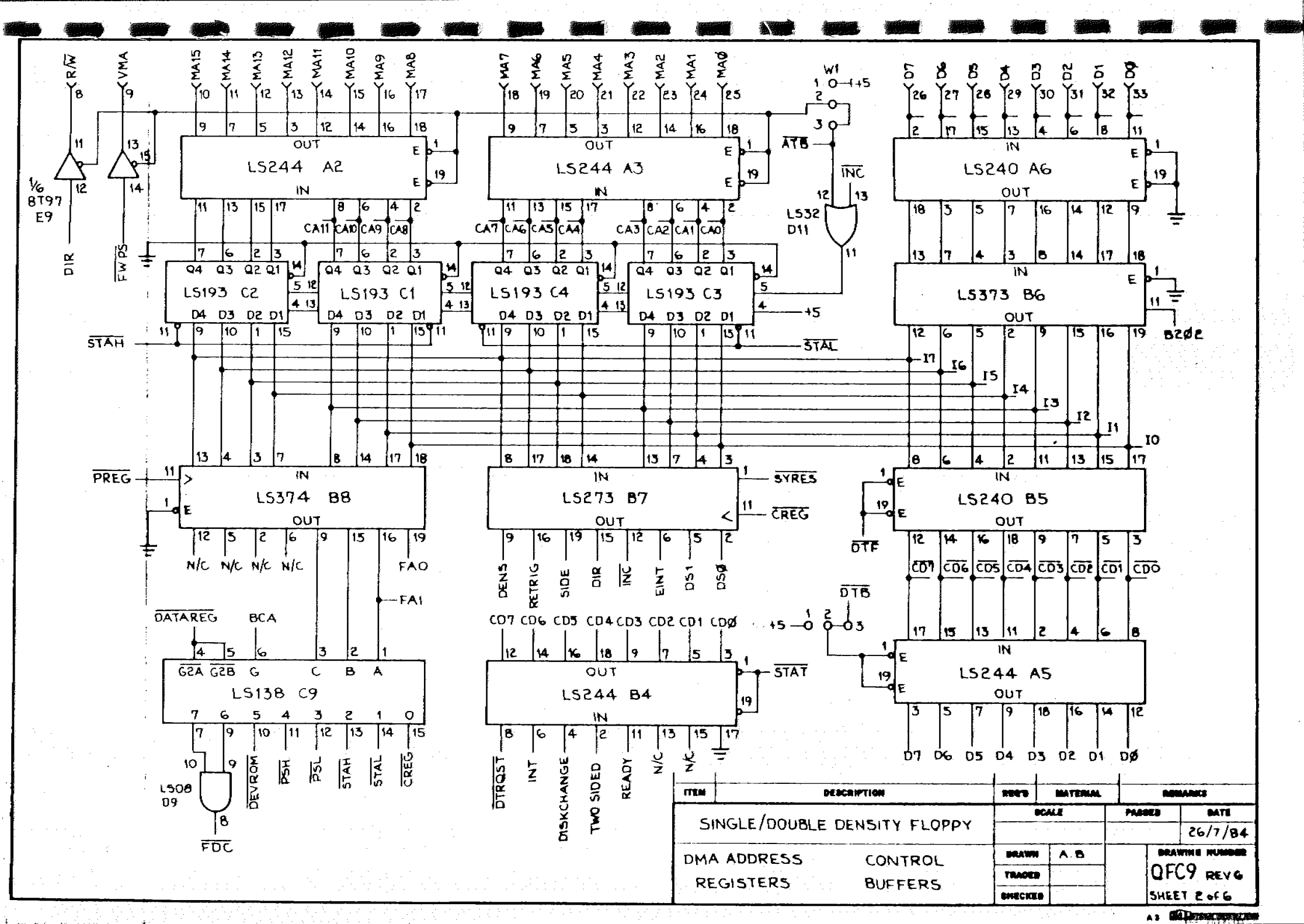
9.10.1 Card Cage removal.

1. Disconnect mains power.
2. Remove top cover, as in section 9.5.
3. Remove the Fan assembly, as in section 9.9.
4. Remove left-hand side cover as in 9.6.
5. Gain access to the Card Cage rear panel by removing the CMI rear panel. Do not completely remove rear panel but disconnect the 6-way mains connector and the 15-way DC power connector that are plugged into the Card Cage rear panel. Each connector has a locking tab that has to be depressed before the the connector can be unplugged.
6. Completely remove the mainframe Front Panel, as in section 9.1.
7. The next step requires all the circuit boards in the Card Cage to be removed. Before proceding, all the circuit boards should have their relative slot number marked, in some way on the circuit board. When all the circuit boards have been marked, remove the circuit boards, as in section 9.2.



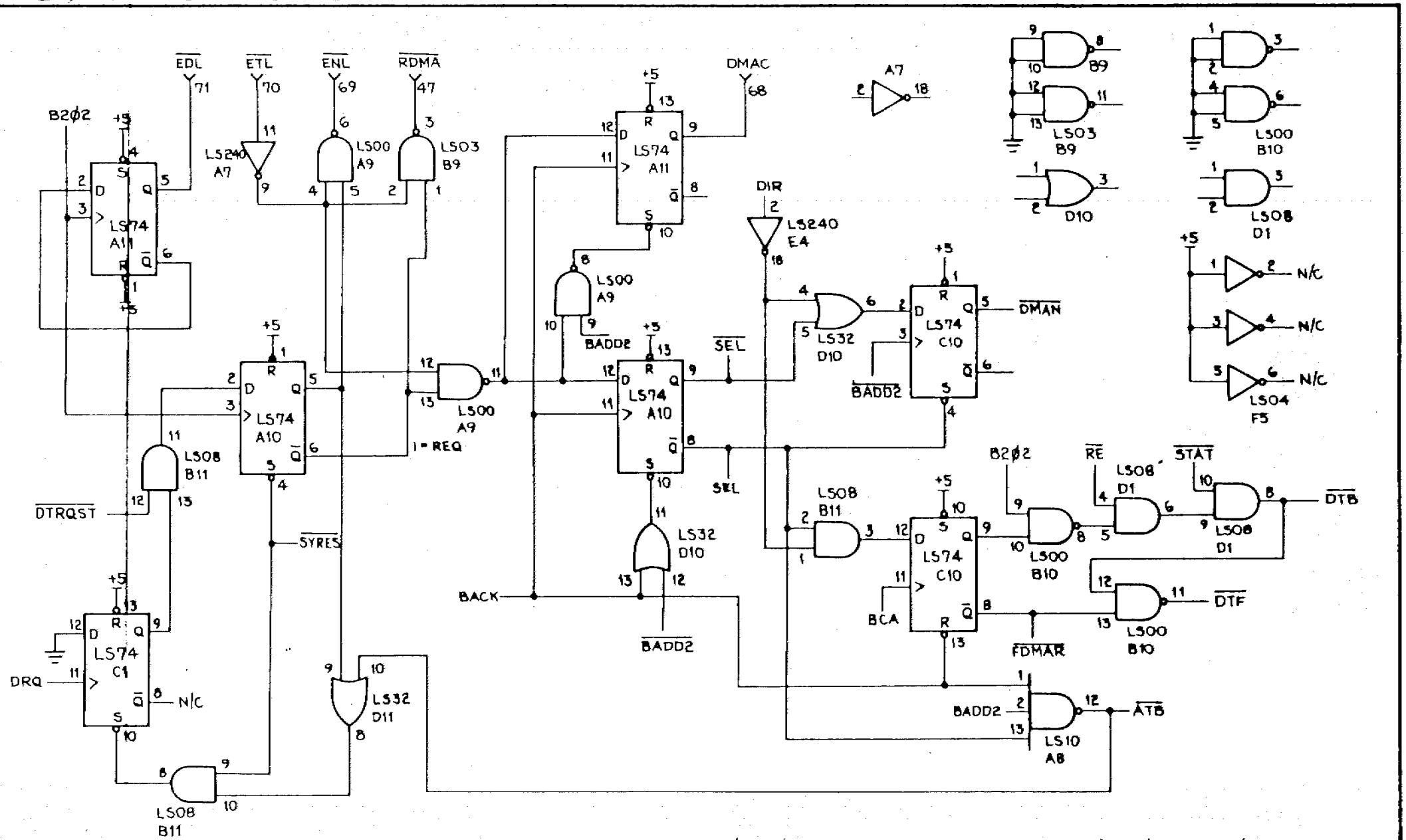
ALL UNMARKED NON INVERTING BUFFERS LS244
" " INVERTING " LS240
WITH PINS 1 AND 19 GROUNDED.

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
SINGLE / DOUBLE DENSITY FLOPPY		SCALE		PASSED / DATE 26/7/84
ADDRESS / CONTROL BUFFERS DEVICER DRIVER ROM.		DRAWN A.B.		DRAWING NUMBER QFC9 REV6
		TRACED		SHEET 1 of 6
		CHECKED		



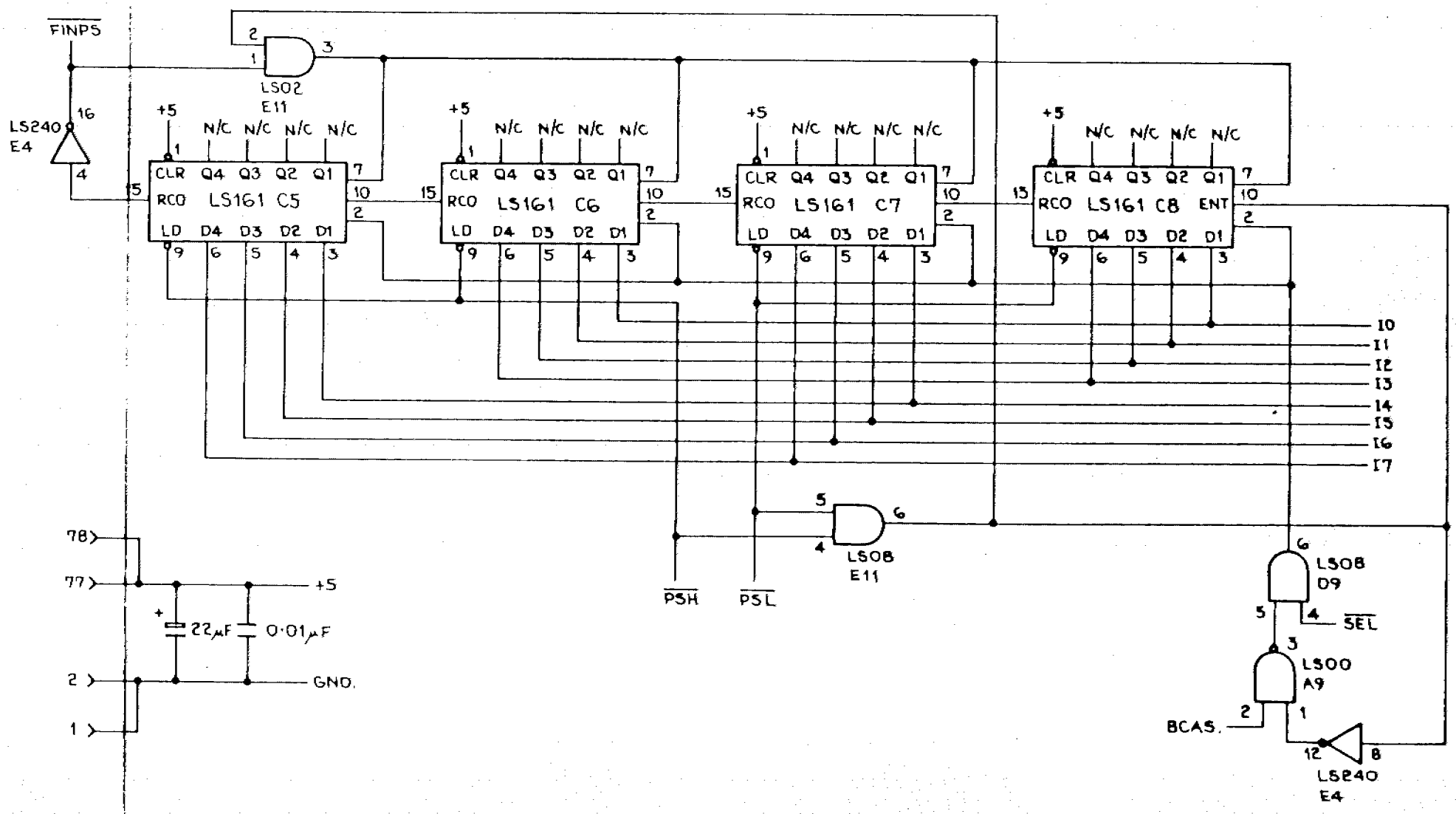
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
SINGLE/DOUBLE DENSITY FLOPPY		SCALE	PASSED	DATE 26/7/84
DMA ADDRESS REGISTERS CONTROL BUFFERS		DRAWN A.B TRACED CHECKED		DRAWING NUMBER QFC9 REV G SHEET 2 of 6

A3



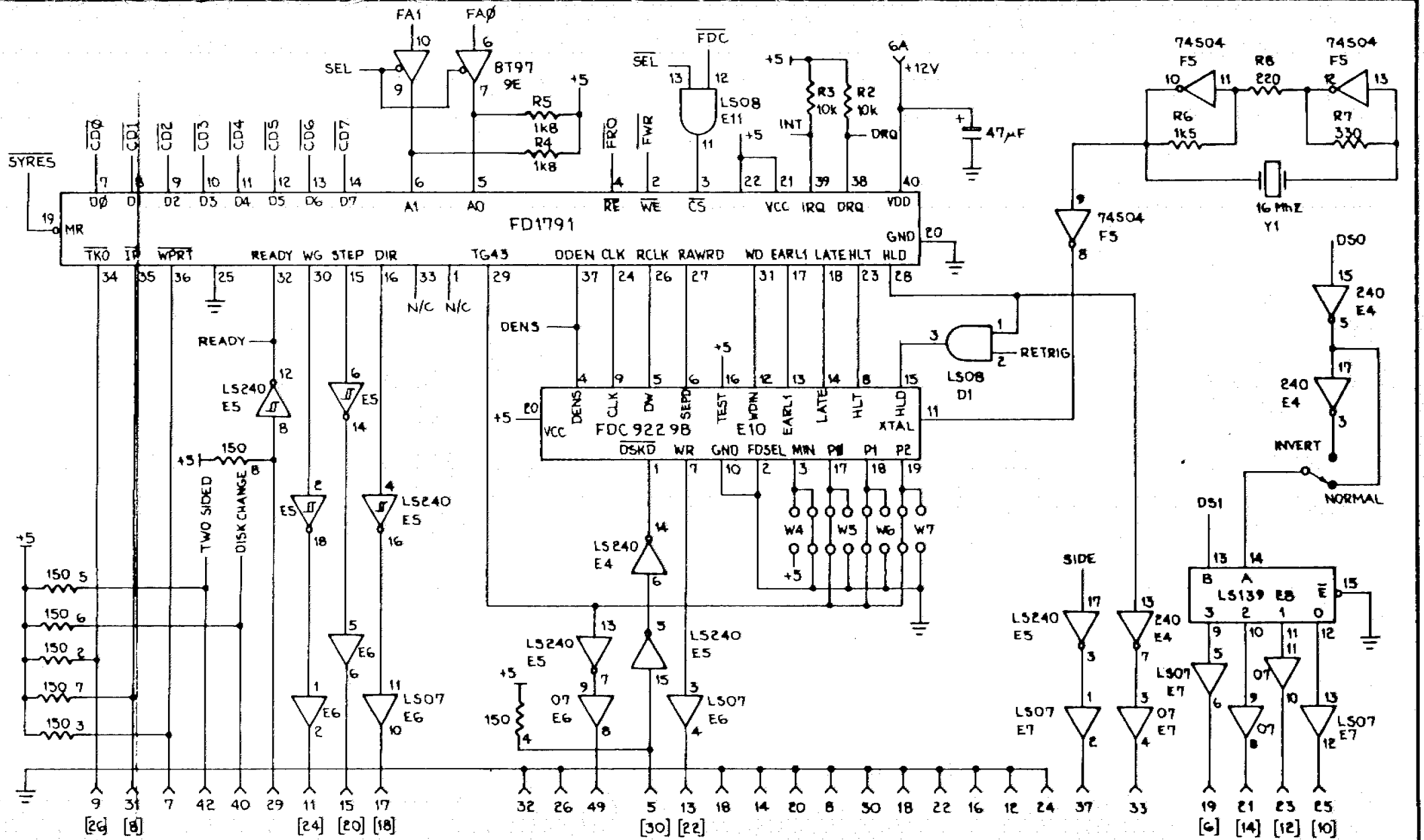
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	SINGLE/DOUBLE DENSITY FLOPPY	SCALE		PASSED / DATE 26/5/84
	DMA LOGIC DAISY CHAIN	DRAWN A.B. / TRACED / CHECKED		DRAWING NUMBER QFC9 REV 6 SHEET 3 of 6

A3



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
SINGLE / DOUBLE DENSITY FLOPPY		SCALE		PASSED / DATE: 24-7-84
BYTE TRANSFER COUNTER		DRAWN: A.B.		DRAWING NUMBER: QFC9 REV 6
		TRACED		SHEET 4 of 6
		CHECKED		

A3



NUMBERS IN [ ] REFER TO 5¼" DISK 34 WAY CONNECTOR WHICH HAS ALL ODD PINS GROUNDED.

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
SINGLE/DOUBLE DENSITY FLOPPY		SCALE	PAGE NO	DATE
FDC/BUFFERS PLL		DRAWN A.B.		DRAWING NUMBER QFC9 REV 6
		TRACED		SHEET 5 of 6
		CHECKED		

A3

1		2	GND
3		4	HDL3
5	READ DATA	6	HDL2
7	WRITE PROTECT	8	
9	TRACK Ø	10	
11	WRITE GATE	12	
13	WRITE DATA	14	
15	STEP	16	
17	DIRECTION	18	
19	DS4	20	
21	DS3	22	
23	DS2	24	
25	DS1	26	
27		28	HDL1
29	READY	30	
31	INDEX	32	
33	HEAD LOAD	34	HDLØ
35	ALT	36	IN USE
37	SIDE SELECT	38	
39		40	DISK CHANGE
41		42	TWO SIDE
43		44	
45		46	
47		48	
49	LOW CURRENT	50	

ITEM | DESCRIPTION | SHEETS | MATERIAL | REMARKS

SINGLE DOUBLE DENSITY FLOPPY

CABLE CONNECTOR SIGNAL 5

41

SCALE | DRAWN A.B. | TRACED | CHECKED

PROVED | DATE 24-7-84

DRAWING NUMBER QFC9 REV C

SHEET 6 of 6

MITSUBISHI FLOPPY DISK DRIVE, M2896-63

SERVICE MANUAL

FAIRLIGHT INSTRUMENTS, FEBRUARY 1985

Revision 2.1

. DISK DRIVE OPTIONING AND ALIGNMENT

.1 Disk Drive Optioning

ptioning may only need to be done if the disk drive has been returned to a itsubishi service centre. If returned to a Fairlight service centre, the drive ill be correctly optioned to perform correctly on the C.M.I.

ɔtion blocks to be shorted - Mitsubishi M2896-63 Rev G

JFC, PS, SE, DC, M2, S2, I, R, IT, MS,
MO, RFA, HR, A, HUN, WP, DS, 2S, RM

ıditional wire link option - Y

.l other option blocks to be left open. See Figure 3.1 for option block ɔcations.

.2 Disk Drive Alignment

.sk drives may require checking to account for any maladjustments which may ɔcur during shipment. This requires the Fairlight Disk Diagnostic Diskette ɔntaining the command **DSKTST.CM.**

ıe disk drive under test should be able to load test programs, however if the ɔndition of the disk drive under test is suspect then another known good disk ·ive should be used to load the test program and used to run the tests on the .ulty disk drive.

2.1 Radial Alignment

cause disk drives utilize double density disk format, radial alignment is itical and is best performed by Fairlight or Mitsubishi. To ascertain whether ive alignment is correct, run the DSKTST command from the Fairlight agnostic disk.

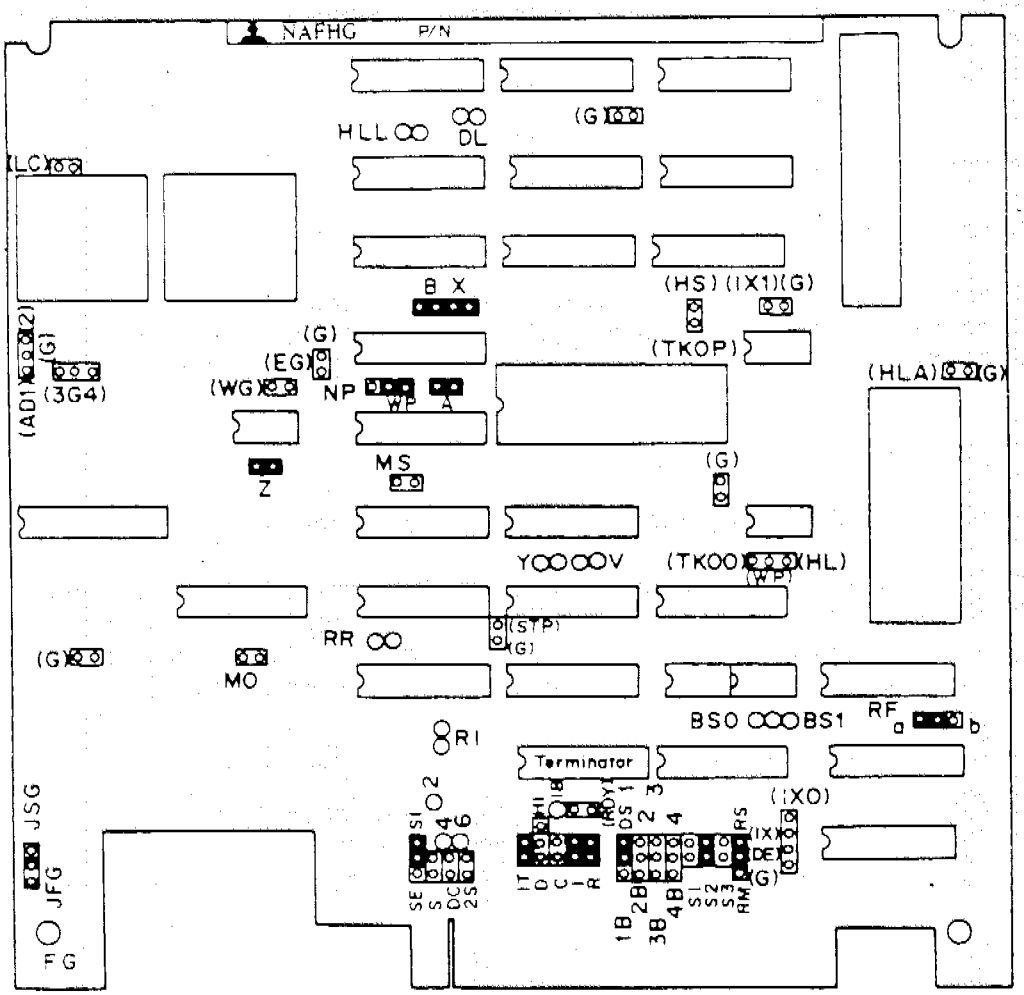


Figure 3.1 Printed Circuit Board Option Block Location

4. DISK DRIVE MAINTENANCE

Under normal circumstances preventive maintenance is not required on the M2896. If severely dirty environments are encountered, an occasional cleaning of the drive may be performed to assure continued reliable performance.

Only basic corrective maintenance is documented here. If it is determined that a disk drive requires more extensive repairs than are described in this section, return the unit to Fairlight Instruments for service. This document should provide sufficient information to determine whether return of the unit is necessary.

4.1 Preventative Maintenance

4.1.1 Visual Check

Visual inspection is the first step in any maintenance operation. Always look for corrosion, dirt, wear, binds, and loose connections. Noticing these items may save downtime later.

4.1.2 Cleaning

Cleanliness cannot be overemphasized in maintenance of the M2896.

Caution: The head/carriage assembly is a factory-adjusted and tested assembly. Do not try to adjust or repair this internal component. Do not, for any reason, clean the read/write heads. To do so would cause severe damage to the head surfaces or head spring supports.

Parts	Observe	Procedure
1. Main Frame	Inspect for loose screws, connectors, switches, etc.	Clean main frame

5. FLOPPY DISK SYSTEM DIAGNOSIS

The Floppy Disk System comprises of the QFC-9 Floppy Disk Controller as well as the disk drives themselves. The first step in servicing the system with an apparently faulty disk system is to establish in what subassembly the fault actually lies.

The general procedure to follow in disk system fault tracing is:

(1) Check all disk system cables, especially the 50 way flat cable for open circuits or shorts and ensure all connections are secure.
(2) Use the system test program CHECK to determine if the fault is in the drive itself (or the diskette) or the disk controller/DMA data transfer system.
(3) If the disk drive is faulty, use DSKTST to further analyse the fault.
(4) Otherwise, refer to the CMI Mainframe manual to trace the fault in the QFC-9 controller.

5.1 Test Program CHECK

Allows checking of;

- Cyclic Redundancy Check (CRC) errors
- Data transfer between memory and disk
- RAM bit corruption errors

Command Syntax

CHECK <UNIT>,<HEXNUM>;<OPTIONS>

where <UNIT> = <COLON><NUMBER>

<HEX DIGIT> = number 1 to 9 and/or letter A to F

e.g., CHECK<return> performs CRC on DRIVE 0.
CHECK :1<return> performs CRC on DRIVE 1.
CHECK :1;V<return> performs CRC on DRIVE 1 with V option.

(1) Disk Integrity Check

Options: none required

This is the default CHECK routine. Entire disk in specified drive is read to check for CRC errors.

5. FLOPPY DISK SYSTEM DIAGNOSIS (continued)

(2) Read Data D.M.A. Verify

Option: V

Reads entire disk in specified drive twice, into separate blocks of memory and verifies data against itself.

(3) Write Data D.M.A. Verify

Options: W,D (May be used together)

The W option creates a file, writes distinctive data to each sector of the file and reads each sector of the file back, twice, into different areas of memory for verification. All unfree disk space will be allocated to the file.

The D option is a destructive (to the disk contents) test which writes a unique "ADD -29" pattern to each sector in an interleaved fashion, reads it back, and verifies the data.

Interleaving of blocks ensures track boundaries are continually being crossed. A delay can be introduced using the "T" option (see below) to isolate head-load timing problems.

(4) Other Options

Option	Use with	
R	W	use random number pattern instead of "29" pattern
P=XX	W	use pattern XX where XX = <hex number> write the pattern to disk, read back and verify
E=XX	all	print error if total recoverable disk errors exceed XX where XX = <hex number>. Default value is 0.
T=XX	all	delay XX*10 ms. after a read/write where XX = <hex number>
C	all	test continously alternating between 'add-29' and a random number pattern
L	all	all error messages printed on printer

5. FLOPPY DISK SYSTEM DIAGNOSIS (continued)

(5) Error messages

(a) Disk Read/Write Errors
These are of the form;

**PROM I/O ERROR -- STATUS = <status byte> AT h DRIVE i - PSN j

where h is not significant
i = drive number
j = physical sector number at which the error occurred

and the status byte can be interpreted as follows:

31 data C.R.C. error
32 disk is write protected
33 disk is not ready for some reason
34 deleted data address mark read
35 abnormal command termination
36 invalid sector address
37 seek error (track not found)
38 data mark read error
39 address mark read error

(b) Verify Errors

When a verify error is encountered the offending disk sector is re-read into the QDOS sector buffer and matched against system RAM to determine where the error came from. The program then reports the corresponding address in RAM, the data expected, the erroneous data, the physical sector number of the disk where the error occured, and the byte offset within the sector.

(6) Termination

Test is terminated by -
ESC key (sets system error status word)
More then 20 errors logged
User supplied iteration counter expired (default 1)

System error status word will be set if any error condition has been reported.

5.2 Test Program DSKTST

DSKTST comprises of five main test routines and a number of utility commands. The main routines are as follows -

#1 Write/read test	(destructive)
#2 Read C.R.C. test	(non-destructive)
#3 Worst case seek test	(non-destructive)
#4 Worst case data pattern R/W	(destructive)
#5 Sector/drive uniqueness	(destructive)

NOTE: DESTRUCTIVE TESTS WILL OVERWRITE THE DISKETTE IN THE DRIVE UNDER TEST WITH A 'TESTING PATTERN'.

Tests can be run separately or in destructive/non-destruct groups by typing as follows -

DN,(0 or 1 or B) [,X]<return> (Do all non-destruct tests)

DD,(0 or 1 or B) [,X]<return> (Do all destructive tests)

ST#<tests>,(0 or 1 or B)[,X]<return>
where <tests> = up to 10 test numbers separated by '-'

The extended test option X accumulates error counts over a number of passes.

ESC key will abort test in progress.

Typing OS<return> will return the user to QDOS and reboot the system.

Examples: DN,0<return> does all non-destructive tests on drive 0 only.

ST#1-3-5,B,X does tests 1,3 and 5 on both drives with error count accumulation.

If stop on error option is selected (in answer to a prompt) the user may choose -

C continue
L loop
R reset stop on error

if an error stop occurs.

5. FLOPPY DISK SYSTEM DIAGNOSIS (continued)

5.2.1 Error reporting

Error printouts take the following form :

<drive no.> <error type> <track no> /<physical sector no> <*>

Presence of '*' indictes a "hard" disk error,

e.g. 1 E3 1F /0325 *

means :- drive no 1
error type 3 (E3)
track no 1F
p.s.n 0325
error was not recoverable on retry (*)

If after three retries the error persists, it will be logged as a hard error (indicated by *).

Error types are as follows (per QDOS ROM codes) :-

E1 data CRC error
E2 disk is write protected
E3 disk is not ready for some reason
E4 deleted data address mark read
E5 abnormal command termination
E6 invalid sector address
E7 seek error (track not found)
E8 data mark read error
E9 address mark read error

Additional error types are :-

E@ data read back is not the same as data written

Additional error types from the drive uniqueness test are :-

EA body of data buffer is not zero after test data
EB unique data for this drive/sector is incorrect.

5. FLOPPY DISK SYSTEM DIAGNOSIS (continued)

5.2.2 Error Graphs

Errors may be summarised by use of the 'PG' command. This summary plots the track no. as the vertical ordinate and the number of errors as the horizontal ordinate.

A horizontal line may contain up to 11 error types (codes) with each character representing (n*horizontal scale) errors.

The error graph is divided into two blocks. The left hand block relates to drive 0 errors, the right hand block to drive 1.

The graph is printed starting at the first track with errors logged and finishes with the last track with errors logged.

To stop the display rolling off the screen, <control W> can be used to stop printing. Subsequent carriage returns will print a little at a time, an escape will terminate the 'PG', and any other character will resume continuous printing.

In the case of double sided systems, each disk 'cylinder' is considered as two tracks, so even track numbers correspond to side 0 of the disk and odd track numbers correspond to side 1.

5.2.3 Utility Commands

Commands for utility programmes are as follows

HD,d,hhhh	Head load timing test on drive d at speed hhhh (100 mS = D8F0)
IX,d	Index sensor alignment test on drive d. t1=tk 1. t2=tk 76.
AT,d,s	Read data amplitude test on drive d. s is optional side select (0 or 1). t1=tk 0. t2=tk 76.
RA,d,s	Radial alignment test on drive d. s is optional side select (0 or 1) t1=0-38. t2=77-38. t3=39-38. t4=37-38.
AZ,d,s	Head azimuth test on drive d. s is optional side select. t1=0-76. t2=75-76.
TO,d	Track zero sensor alignment test on drive d. t1=1-2 lp. t2=0-1 lp. t3=0-2 lp.
SK,d,s	Head skew test on drive d. s is optional side select (0 or 1). t1=1-76 lp.
RS,d,hhhh	Read sector hhhh from drive d to buffer
WS,d,hhhh	Write buffer to sector hhhh on drive d
DB	Display buffer in hex and ascii
FB,hhhh	Fill buffer with repeating pattern hhhh

The running test may be aborted by escape key.
The next test of the sequence is entered by depressing space key.
Tests followed by letters "lp" move head between tracks shown.

Some tests require the appropriate alignment diskette and ask that it be inserted. Other tests require a scratch diskette and ask that it be inserted.

Typing OS<return> will return the user to the operating system (reboot).