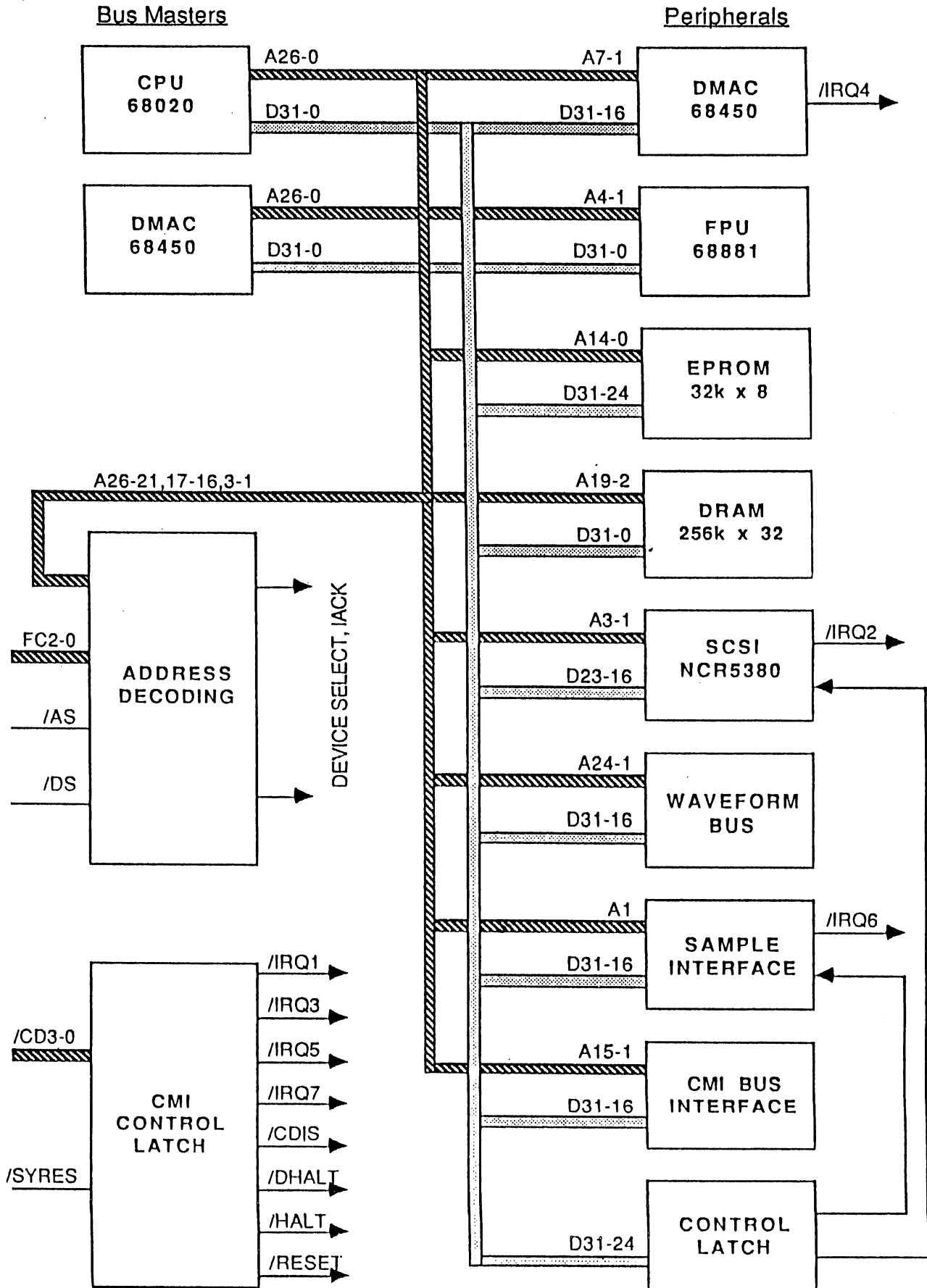
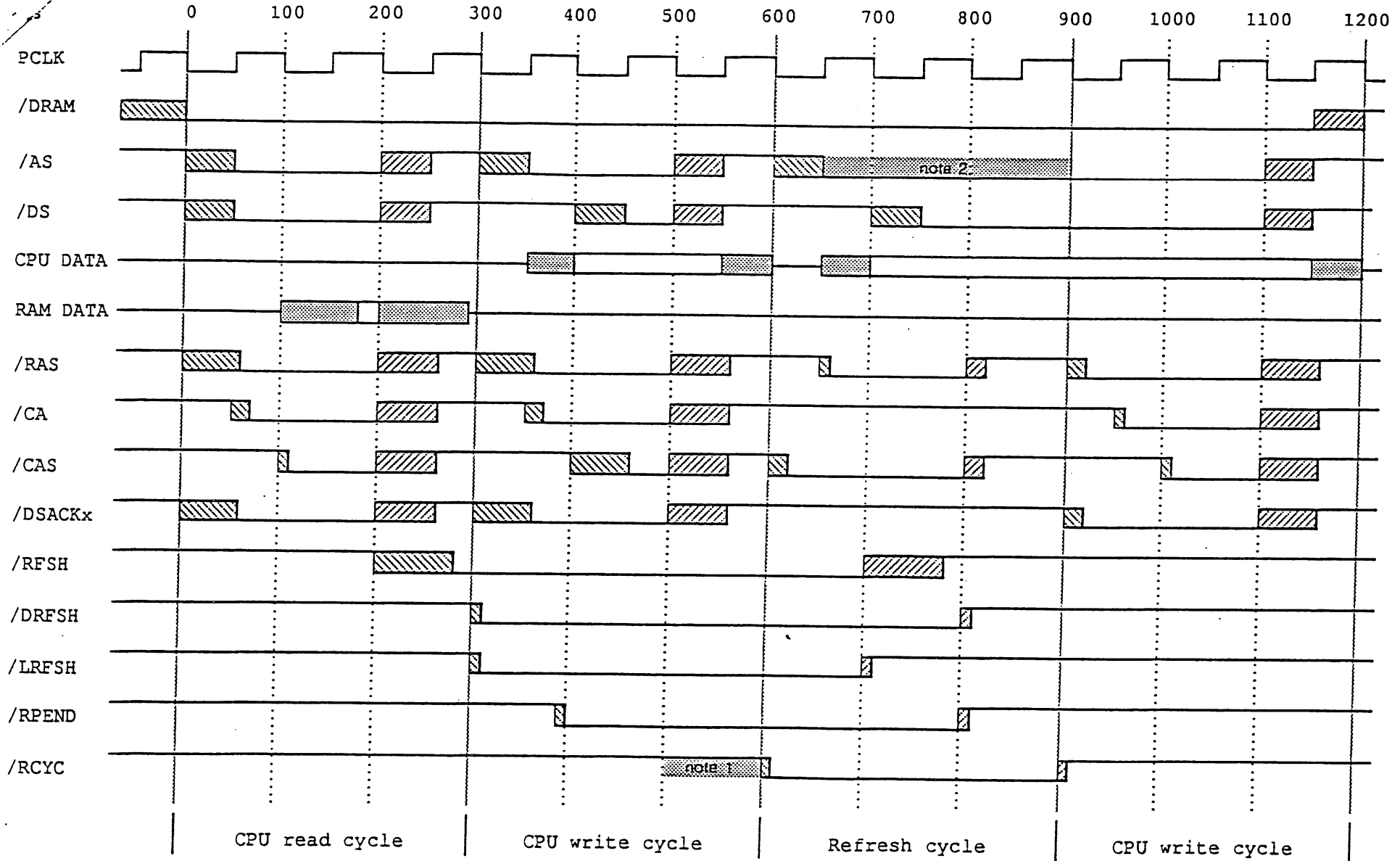


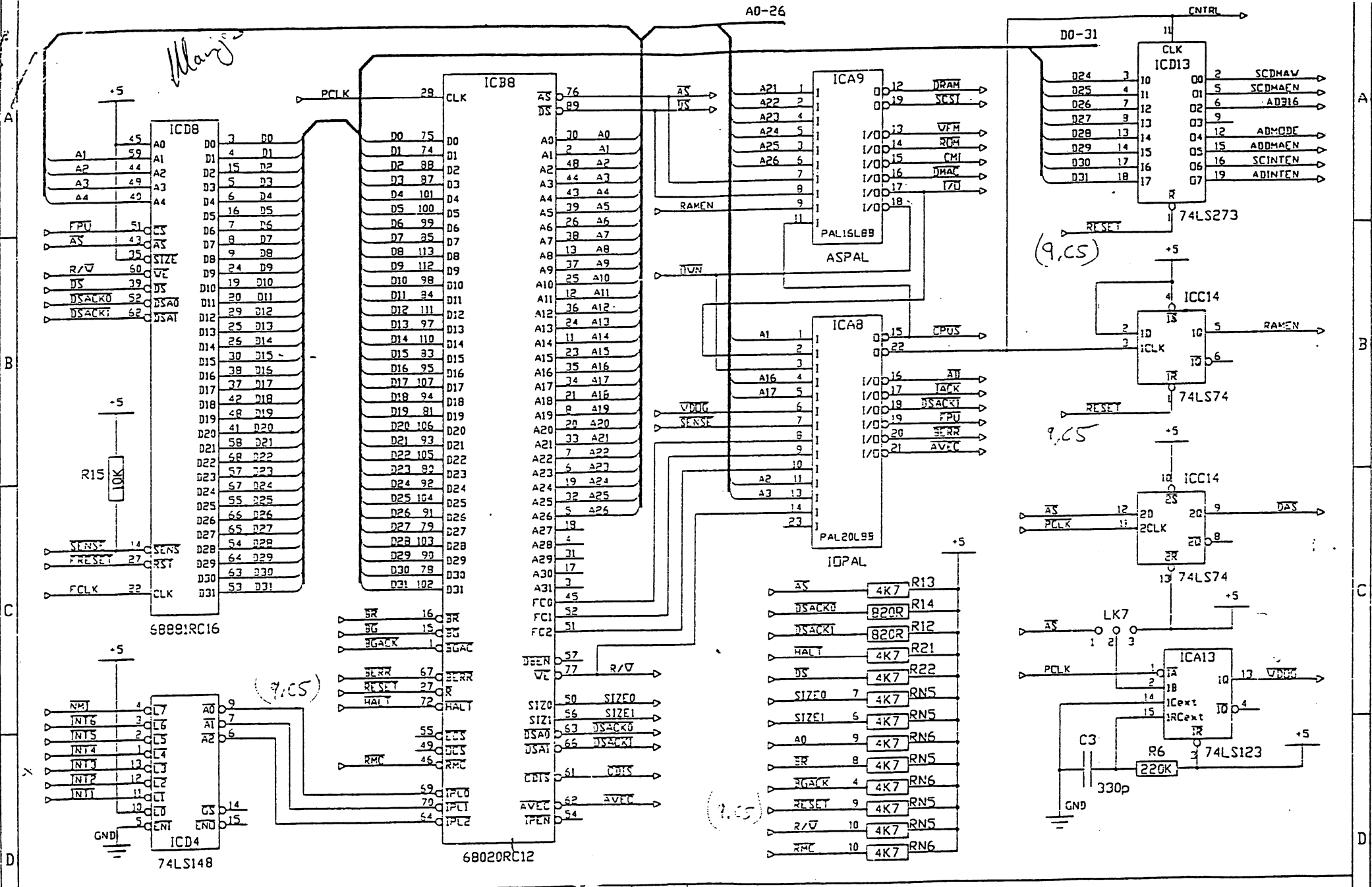
CMI-41 Internal Bus Devices



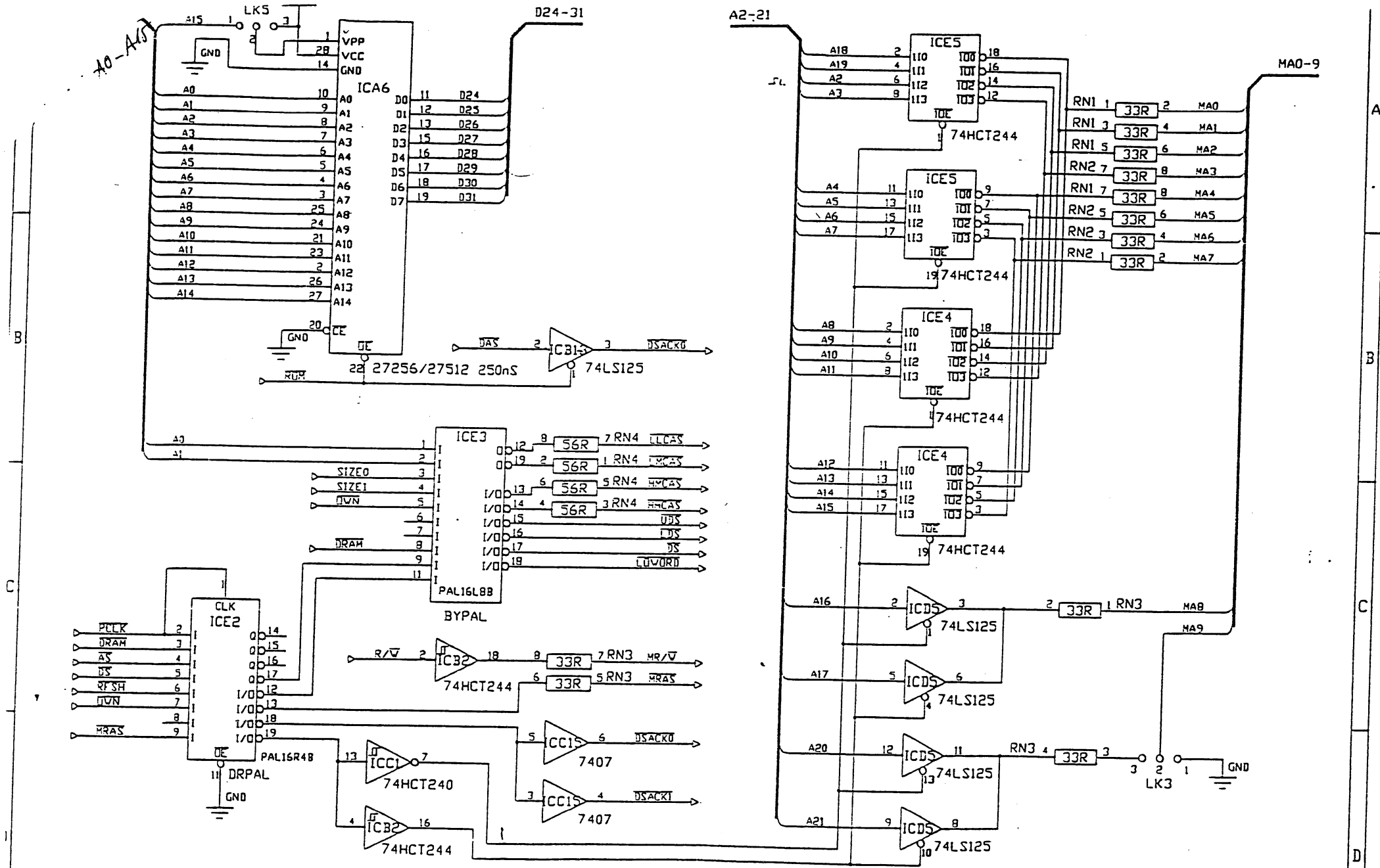
CMI-41 Dynamic RAM Timing (DRPAL)



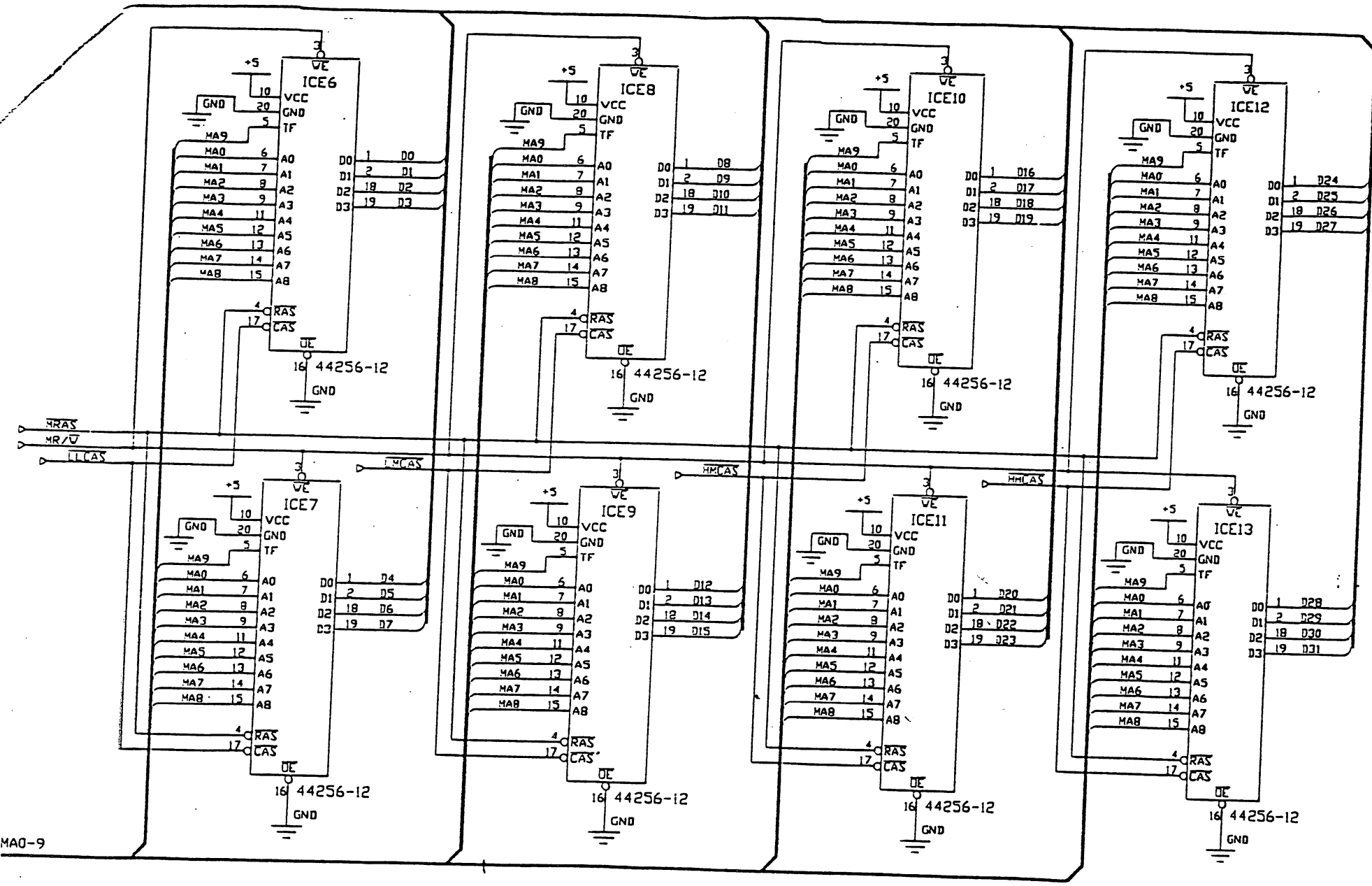
- Notes:
1. Refresh cycle delayed by current CPU cycle.
 2. CPU cycle pre-empted by pending refresh cycle (up to 3 wait cycles inserted).
 3. This diagram assumes 12MHz 68020, 120nS DRAMs, 15nS PAL.



CPU, FPU, INTERRUPTS, ADDRESS DECODING, WATCHDOG, CONTROL LATCH			FAIRLIGHT INSTRUMENTS		
ZONE	DESCRIPTION	ISSUE	DATE	APP'D	DRAWING-NO
DATE	4th Nov 1987	TITLE	CMI-41 rev 1		
DESIGN BY	AJCannon	SHEET-NO		1 OF 10	ISSUE
1	2	3	4	5	6



DYNAMIC RAM CONTROL, EPROM					FAIRLIGHT INSTRUMENTS					
ZONE	DESCRIPTION				ISSUE	DATE	APP'D	DRAWING-NO		
DATE	4th Nov 1987	TITLE						CMI-41 rev 1		
DESIGN BY	AJCannon	WAVEFORM SUPERVISOR						SHEET-NO	2 OF 10	ISSUE
1	2	3	4	5	6	7	8	9	10	11



DYNAMIC RAM ARRAY

DESCRIPTION

ISSUE DATE APP'D

FAIRLIGHT INSTRUMENTS

DATE 5th Nov 1987
DESIGN BY AJCannon

TITLE
WAVEFORM SUPERVISOR

DRAWING-NO

CMI-41 rev 1

SHEET-NO
3 OF 10

ISSUE
1

1

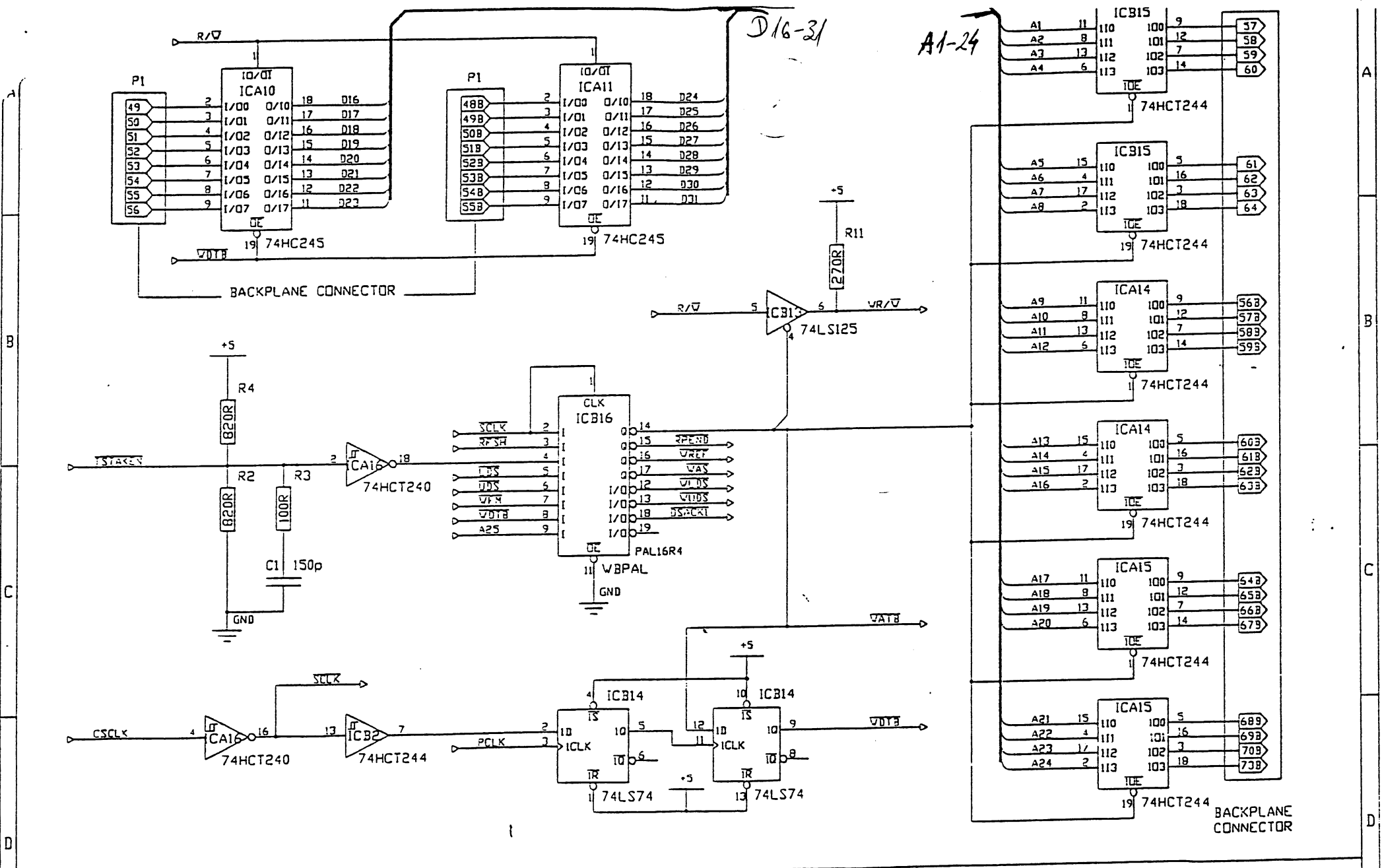
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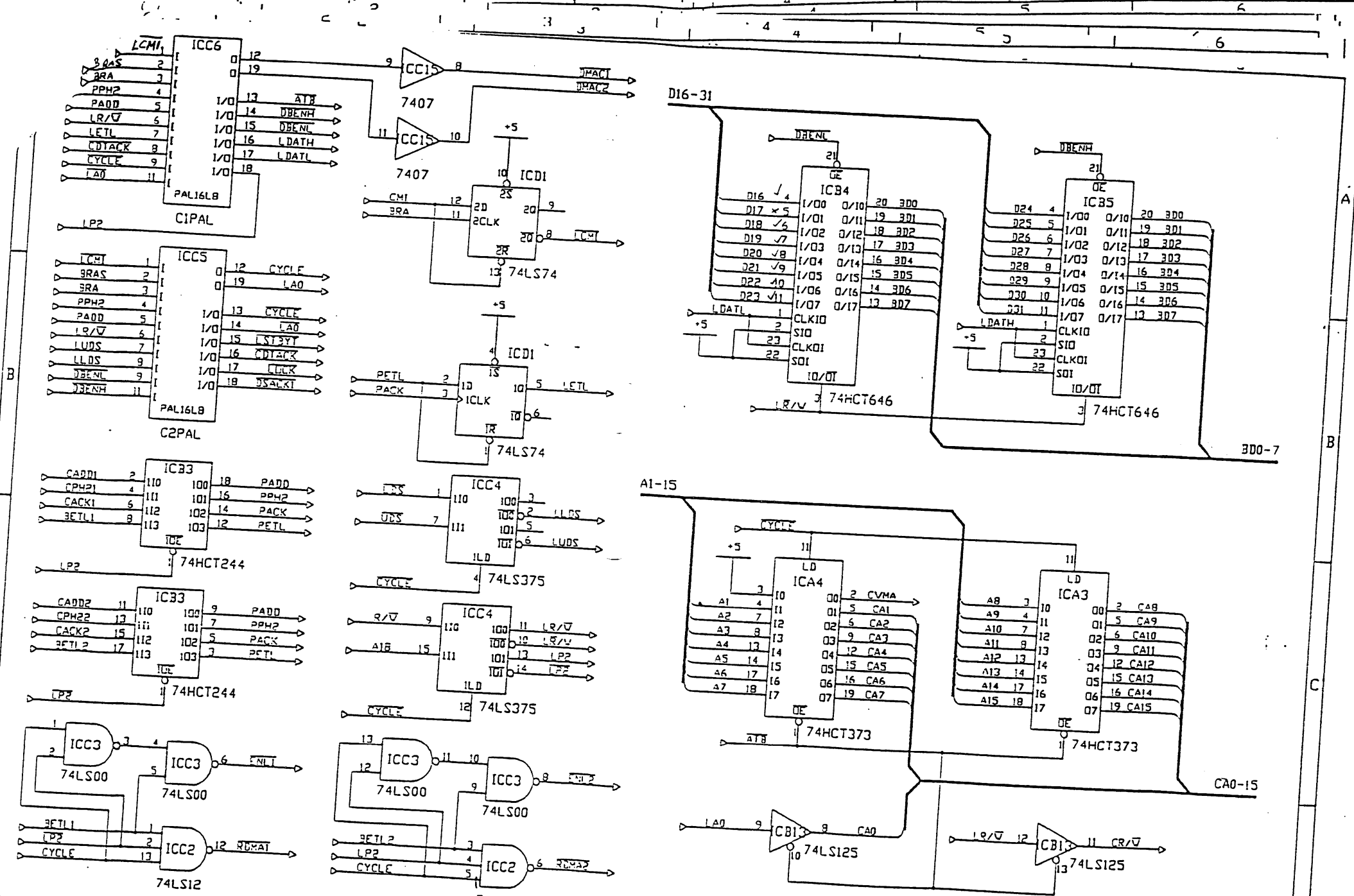
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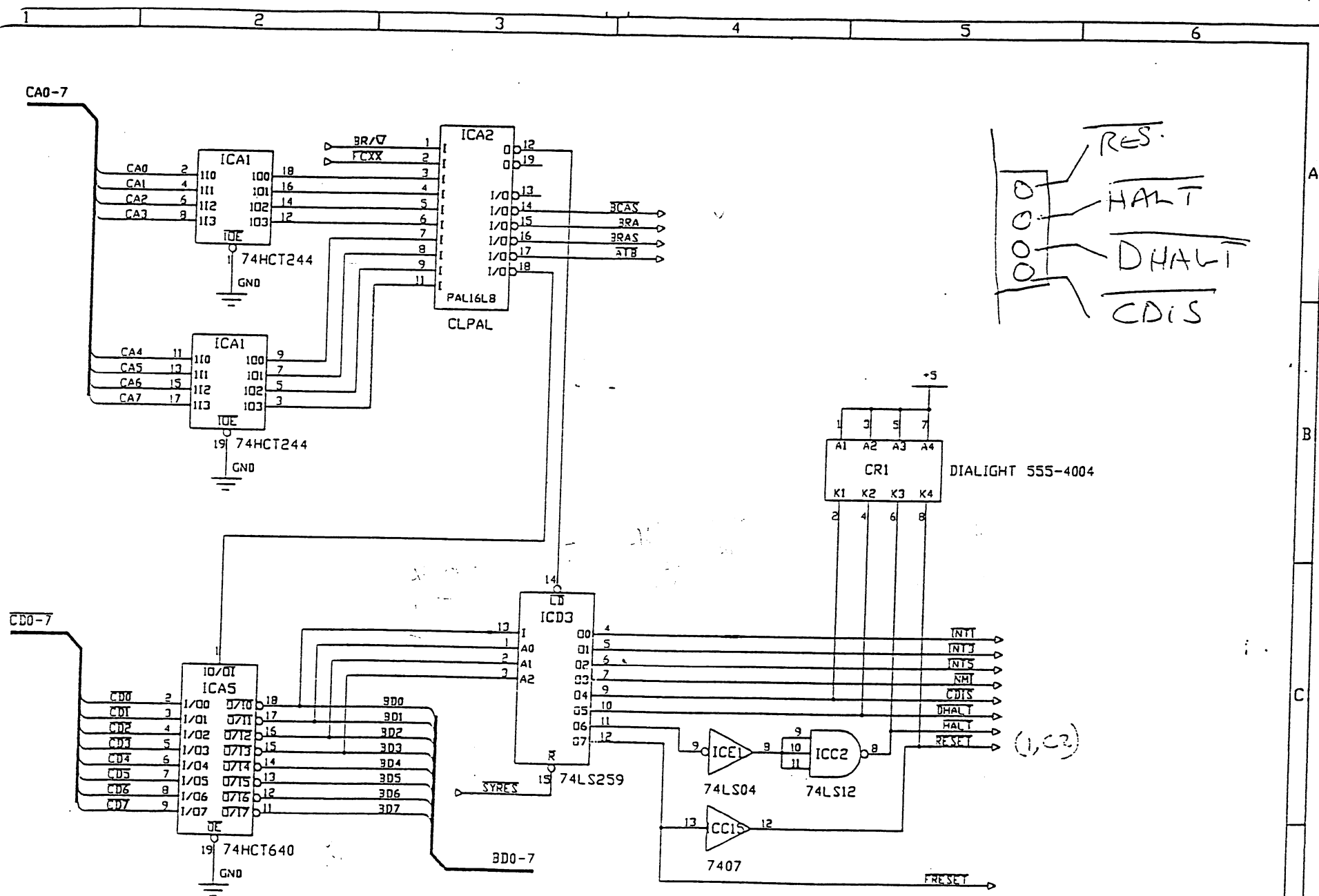
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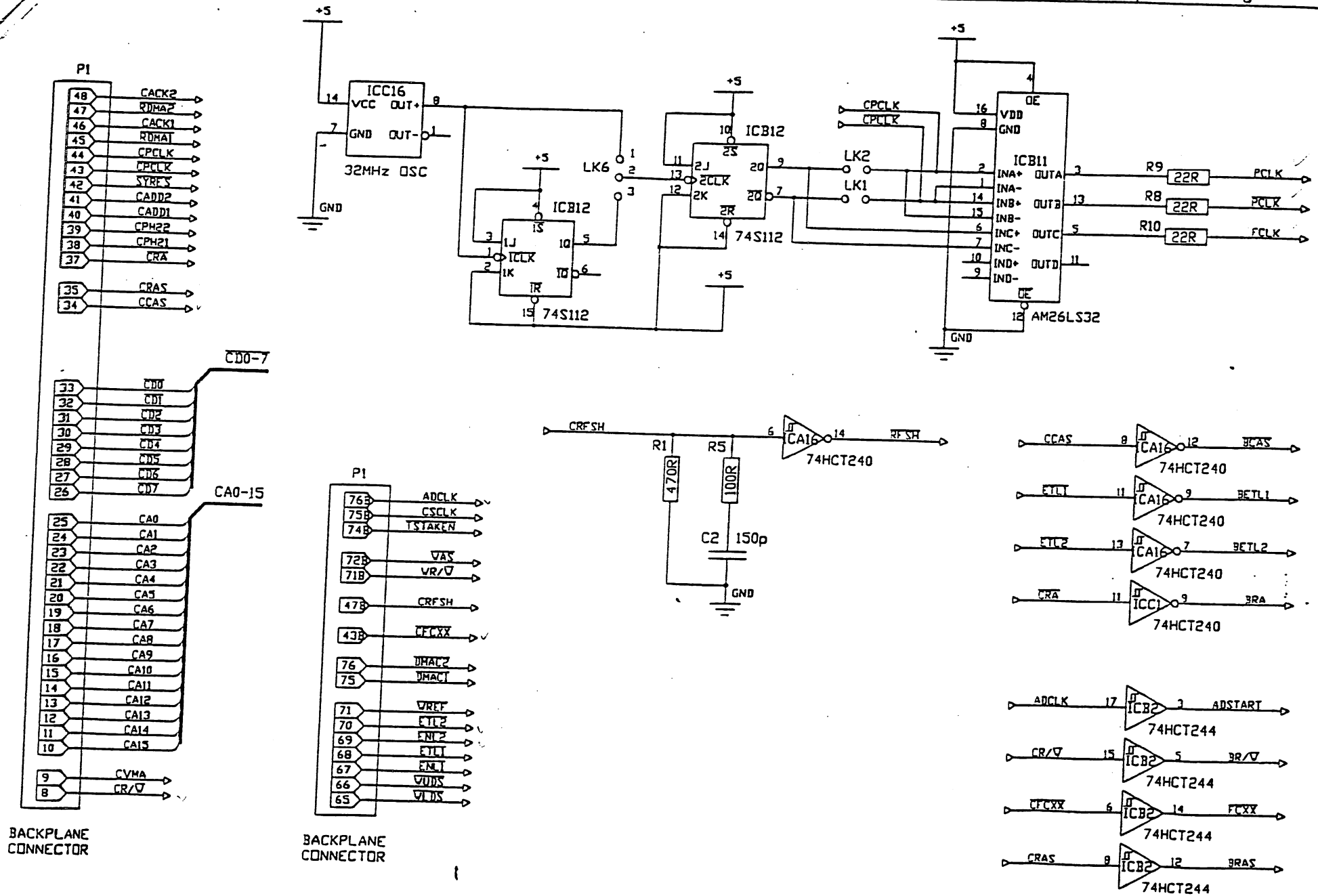
WAVEFORM BUS INTERFACE		FAIRLIGHT INSTRUMENTS		
ZONE	DESCRIPTION	ISSUE	DATE	APP'D
DATE	5th Nov 1987	DRAWING-NO		CMI-41 rev 1
DESIGN BY	AJ Cannon	SHEET-NO		6 OF 10
WAVEFORM SUPERVISOR		ISSUE		1
1	2	3	4	5
		6		



ZONE		CHM BUS INTERFACE				
DATE		DESCRIPTION		ISSUE	DATE	APP'D
6th Nov 1987						



CONTROL LATCH LEADS		ISSUE	DATE	APP'D	FAIRLIGHT INSTRUMENTS
ZONE	DESCRIPTION				
DATE	6th Nov 1987	TITLE	WAVEFORM SUBOVERSPO	DRAWING-NO	SHEET-NO
					ISSUE



BACKPLANE CONNECTOR

BACKPLANE CONNECTOR

ZONE		DESCRIPTION	ISSUE	DATE	APP'D	FAIRLIGHT INSTRUMENTS
DATE 6th Nov 1987		TITLE				
DESIGN BY		WAVEFORM SUPERVISOR				